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# A novel autozeroing technique for flash Analog-to-Digital converters

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ABSTRACT

This paper presents a new autozeroing technique that combines very high speed operation, low power consumption and low input switching interferences. This technique has been applied to the design and implementation of a 6-bit 0.13 μm CMOS flash Analog-to-Digital converter for Ultra-Wide Band applications. Simulation results show 5.76-bit at 1 GS/s with a power consumption of only 182 mW, validated with experimental measurements carried out with 3-bit circuit tiles of the 6-bit flash A/D converter.



## 1. Introduction

Flash Analog-to-Digital converters (ADCs) are an attractive option for present communication systems, especially in wireless standards. The scaling-down of technologies allows very complex signal processing at a high speed and moderate power consumption, opening the way for high speed communications in mobile and portable systems. Many applications, such as Ultra-Wide Band (UWB) transceivers, have recently created a great demand of high speed ADCs. In addition to this, low/medium resolution flash ADCs can also be implemented as a part of Time-interleaving (TI) or Successive-Approximation-Register (SAR) ADCs working at very high-frequencies.

In present technologies, flash ADCs performances are limited by errors caused by process variations. A common solution to this problem is to place a chain of gain stages in front of the comparators, but the large number of amplifiers leads to high area and power consumption. A popular technique to reduce the number of such front-end amplifiers is capacitive interpolation with autozeroing [1,2]. The main advantages of the capacitive interpolation technique are [1]

- No over range comparators or static averaging terminations are required.
- There is no need for an external Sample-and-Hold (S&H) as the autozeroing technique inherently provides a distributed S&H.

However, the implementation of this technique has some important drawbacks [3]

- The switched capacitors at the input produce interferences at the input node, leading to significant switching noise.
- The need of two non-overlapping clock phases limits the maximum operation frequency of the converter.

A new autozeroing technique applied to the design of a flash ADC for UWB applications is presented in this paper. The proposed scheme does not have capacitors at the ADC input, reducing the input loading and thus the power consumption of the previous receiver blocks.

Another advantage of the proposed scheme is that the amplifiers do not charge any non-parasitic capacitor, except for the first amplification stage, increasing the amplifiers' bandwidth for the same power consumption. Moreover, the proposed technique requires only a single clock signal instead of two non-overlapping ones, allowing the amplifiers to have the whole clock period to settle their outputs. As a result, the bandwidth requirements of the amplifiers are relaxed, further reducing the power consumption. On the other hand, it requires periodical refresh cycles to perform a foreground calibration, which should be applied during dead times.

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## 2. Proposed implementation

The autozeroing technique is widely used in interpolation-based flash ADCs to reduce the offset of the comparators. A conventional autozeroing solution is shown on the circuit in Fig. 1, whose operating principle is roughly described here.

During the first clock phase ($\phi 1$), the difference between the reference voltage and the amplifier offset is stored in capacitor $C$; in the second clock phase ($\phi 2$) this value is subtracted from the input signal and applied to the open-loop amplifier. As stated before, this technique suffers from important drawbacks (such as input switching interferences or the existence of two non-overlapping clock phases) which reduce the conversion rate.

In this paper, a new autozeroing technique to solve these problems is proposed. The amplification stage (Fig. 2a) with the proposed autozeroing technique (Fig. 2b) operates in two different modes: *Calibration Mode* (*CAL*='1') and *Normal Operation Mode* (*CAL*='0').

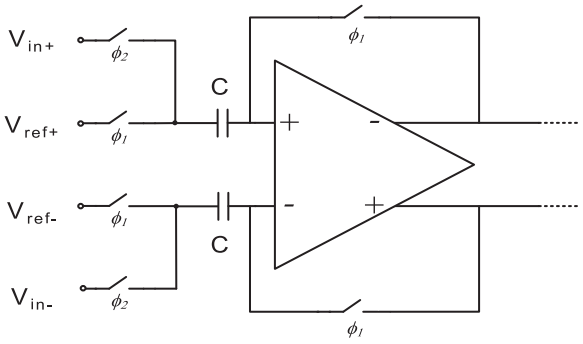


**Fig. 1.** Input stage of the conventional amplifier with autozeroing technique.

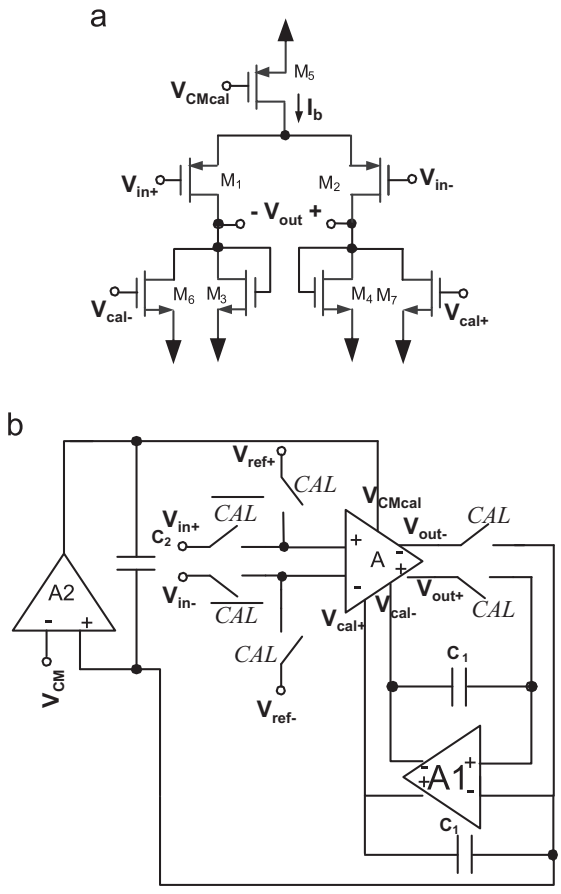


**Fig. 2.** (a) Main amplifier and (b) amplification stage with the proposed autozeroing technique.

The differential pair ($M1$,$M2$) with the diode-connected load ($M3$,$M4$) builds up the main high frequency amplifier, which has a low-gain $A$. Transistors $M6$ and $M7$ are used to compensate its offset error $V_{off}$. The common mode voltage is controlled by means of the gate terminal of $M5$. There are two additional high-gain low-frequency amplifiers in Fig. 2b: $A_1$ implements a feedback loop to compensate for the offset error of the main amplifier, and $A_2$ implements the common mode control. As both feedback loops are simultaneously active, the common mode compensation can be performed using only one output of the main amplifier. The switches shown in Fig. 2b have been implemented using nMOS transistors.

Next, the two operation modes of the proposed amplification stage with the proposed technique are explained.

### 2.1. Calibration mode

In this mode, the control signal *CAL* is at a high level and the differential reference voltage ($V_{ref+}-V_{ref-}$), obtained from a resistor ladder, is applied to the inputs of the main amplifier. It can be noted that if $V_{ref}$ is too large, the linearity of the amplifier can be compromised. To minimize this drawback, in the proposed design the dynamic signal range at the input of the amplifier has been limited to 400 mV, with a 1.2 V supply. As a result of the negative feedback loop implemented by the amplifier $A_1$, proper values for the gate voltages of $M_6$ and $M_7$ are generated so that the differential input of $A_1$ is close to zero. This will result in a suitable value for the input offset which will be maintained during normal operation. Then, the equivalent input offset voltage of the main amplifier is set to

$$(V_{ref+}-V_{ref-})+\frac{1}{A}\left[V_{off1}+\frac{(V_{ref+}-V_{ref-})+V_{off}}{A_1}\right]\approx(V_{ref+}-V_{ref-}) \qquad (1)$$

where $A$ and $V_{off}$ are the gain and offset voltage (without calibration) of the main amplifier, $V_{off1}$ and $A_1$ are the offset voltage and gain of amplifier $A_1$, respectively. A study of the input offset of the amplifiers has been performed by means of Monte Carlo simulations, taking into consideration both process variations and mismatch effects. Obtained results (for $N=300$ iterations) show a significant improvement of the input offset; for the first stage, input offset is reduced more than a 2x factor applying calibration. In the last stage—the most sensitive to mismatch-values of expected mean and standard deviation are reduced from 0.5 mV and 10 mV to 10 μV and less than 1 mV, respectively.

### 2.2. Normal operation mode

Once the calibration phase has finished, the *CAL* signal goes down, so that the differential signal coming from the previous stage (or the input signal, for the case of the first stage) is applied to the inputs of the main amplifier.

During this phase, capacitors $C_1$ and $C_2$ are disconnected from the amplifier outputs and their respective feedback loops remain open; therefore, it is possible the operation of the amplifier at very high frequency. While the charge losses in $C_1$ and $C_2$ (caused by the leakage currents in the switches) are not significant, the stage can remain calibrated (measures show the resolution begins to fall near 800 ns). The values of $C_1$ and $C_2$ should be large enough (0.5 pF) to maintain the calibration during a long time, which is possible because the capacitors are not in the signal path. On the other hand, switches in the feedback loop are of minimum size to minimize charge injection. Post-layout simulation results show an