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Design of two Low-Power full adder cells using GDI structure and hybrid CMOS logic style

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ABSTRACT

Full adder is one of the most important digital components for which many improvements have been made to improve its architecture. In this paper, we present two new symmetric designs for Low-Power full adder cells featuring GDI (Gate-Diffusion Input) structure and hybrid CMOS logic style. The main design objectives for these adder modules are not only providing Low-Power dissipation and high speed but also full-voltage swing.

In the first design, hybrid logic style is employed. The hybrid logic style utilizes different logic styles in order to create new full adders with desired performance. This provides the designer with a higher degree of design freedom to target a wide range of applications, hence reducing design efforts. The second design is based on a different new approach which eliminates the need of XOR/XNOR gates for designing full adder cell and also by utilizing GDI (Gate-Diffusion-Input) technique in its structure, it provides Ultra Low-Power and high speed digital component as well as a full voltage swing circuit.

Many of the previously reported adders in literature suffered from the problems of low-swing and high noise when operated at low supply voltages. These two new designs successfully operate at low voltages with tremendous signal integrity and driving capability. In order to evaluate the performance of the two new full adders in a real environment, we incorporated two 16-bit ripple carry adders (RCA). The studied circuits are optimized for energy efficiency at 0.13 μm and 90 nm PD SOI CMOS process technology. The comparison between these two novel circuits with standard full adder cells shows excessive improvement in terms of Power, Area, Delay and Power-Delay-Product (PDP).

1. Introduction

Addition is a very basic operation in arithmetic. Subtraction, multiplication, division and address calculation are some of the well-known operations based on addition. These operations are widely used in many VLSI applications, since the full adder cell is the building block of the binary adder, enhancing the performance of the 1-bit full adder is a significant goal and has attracted much attention. A variety of full adders using different logic styles and technologies have been reported in literature [1–5] and they commonly aim at reducing power consumption and increasing speed.

Adder performance affects the arithmetic system as a whole. There are two main ways to improve adder's performance in the literature. One is 'System Level viewpoint' approach which is finding the longest critical path in the ripple adders and then shortens the path in order to reduce the total critical path delay. In most situations, the longest signal path is in the propagation of carry out signals to generate the carry out signal of the most significant bit. Another approach is 'Circuit Design viewpoint' in transistor level, that is, design of high-performance full adder core based on transistor level design skills. At the circuit level, an optimized design is required to prevent any reduction in the output signal, consume less power, have less delay in critical path and be reliable even at low supply voltage as we scale towards nano-meter. Good driving capability under different load conditions and balanced output to avoid glitches is also an important point. Since the full adder cells are duplicated in large numbers, layout regularity, and interconnect complexity are also of importance.

By scaling down the feature size of MOSFET devices in nano-meter, the supply voltage should be scaled down to avoid hot-carrier effects in CMOS circuits. In order to keep and increase the speed of CMOS circuits, the threshold voltage has to be scaled down. However, threshold voltage scaling causes an increase in the standby current. As a result, static power becomes a real contributor to total power in nano-scale circuits and needs an efficient power control [6].

Several different static CMOS logic styles have been proposed to implement Low-Power adder cells [7,8]. Generally they are divided

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into two main categories: classical designs which use only one logic style for the whole full adder design and the hybrid CMOS logic styles that use more than one logic style in their structure.

Complementary CMOS (C-CMOS) full adder [8–11] is an example of classical approach. This full adder is based on the regular CMOS structure with PMOS pull-up and NMOS pull-down transistors. One of its merits is its robust structure against voltage scaling and transistor sizing. This circuit provides full-swing which is essential when utilized in a more complex structure. The layout of the C-CMOS full adder is simple, symmetric and efficient due to the complementary transistor pairs however due to employing number of large PMOS transistors in its structure, the input capacitance is large and also the existence of sized up PMOS transistors has a direct impact on its area.

The complementary pass transistor logic (CPL) [8,9,11,12] full adder with swing restoration is another classical circuit. It has a dual-rail structure with 32 transistors. It provides high-speed, full-swing output and good driving capability due to the output static inverters and the fast differential stage of cross-coupled PMOS transistors. The main drawback of CPL is large power consumption due to existence of a number of internal nodes and static inverters which are the primary source of the leakage and static power dissipation.

The other two full adder designs contain transmission function full adder (TFA) [8,9,13] and transmission gate full adder (TGA) [13,14,20]. These designs are based on transmission function theory and transmission gates. Transmission gate [14,15] consists of a PMOS transistor and an NMOS transistor that are connected in parallel which is a particular type of pass-transistor logic circuit. There is no voltage drop problem but it requires double the number of transistors to design a similar function. TFA and TGA are low power consuming and they are suitable for designing XOR or XNOR gates [8–10,16]. The main disadvantage of these logic styles is that they lack driving capability. When TGA or TFA are cascaded, their performance degrades significantly. Hence, in order to improve its weak driving capability additional buffers are needed. These additional buffers increase the power consumption and chip area [8].

The rest of this paper is organized as follows. Section 2 discusses two previously reported full adder designs in hybrid CMOS logic styles. In Section 3, two new approaches in designing Ultra Low-Power full adder cells using GDI technique [17] and hybrid CMOS logic style are proposed. The proposed full adder cells exhibits low PDP, full-swing operation and excellent driving capabilities. Quantitative evaluation and comparisons of two proposed full adders versus four well known state-of-the-art designs is carried out in a real environment which is a two 16-bit ripple carry adders (RCA) in Section 4 and the new adders displayed better performance as compared to the standard full adders. Finally, Section 5 concludes the paper.

2. Review of two well-known hybrid full adder cells

The hybrid logic style uses different logic styles in order to create new full adders with desired performance. As an example, Hybrid-CMOS full adder [7], shown in Fig. 1, could be mentioned. This circuit utilizes a novel XOR-XNOR design to produce internal signals (Module.1). Module.1 is based on complementary pass transistor logic (CPL) and one inverter. The first half uses only NMOS pass transistors for generating the output. This circuit is inherently fast due the use of high mobility NMOS transistors and fast differential cross-coupled PMOS transistors. The main drawback of this circuit is large power consumption due to the use of CPL structure [8,11] and also an inverter which is the primary source of static power dissipation in nano-scale circuits. In order to implement module.3 (Cout output) this circuit uses four transistors XOR gate [18] and one inverter. As discussed in [7], the first part of module.3 is inherently Low-Power due to its pass transistor structure, but as mentioned in [7], they suffer from lack of driving capability. The output inverter is added in order to improve driving capability in a cascaded situation which simultaneously increases the power consumption and the area. Finally this design uses a new hybrid circuit for implementing module.2 (SUM output). Module.2 uses the Low-Power consuming Transmission Gates and the robust static-CMOS logic style to create a new SUM output. It utilizes ten transistors and possesses the properties of both static-CMOS and Transmission gates logic styles. As discussed in [8], because of employing large PMOS transistors in static-CMOS logic style, the input capacitance is large and also

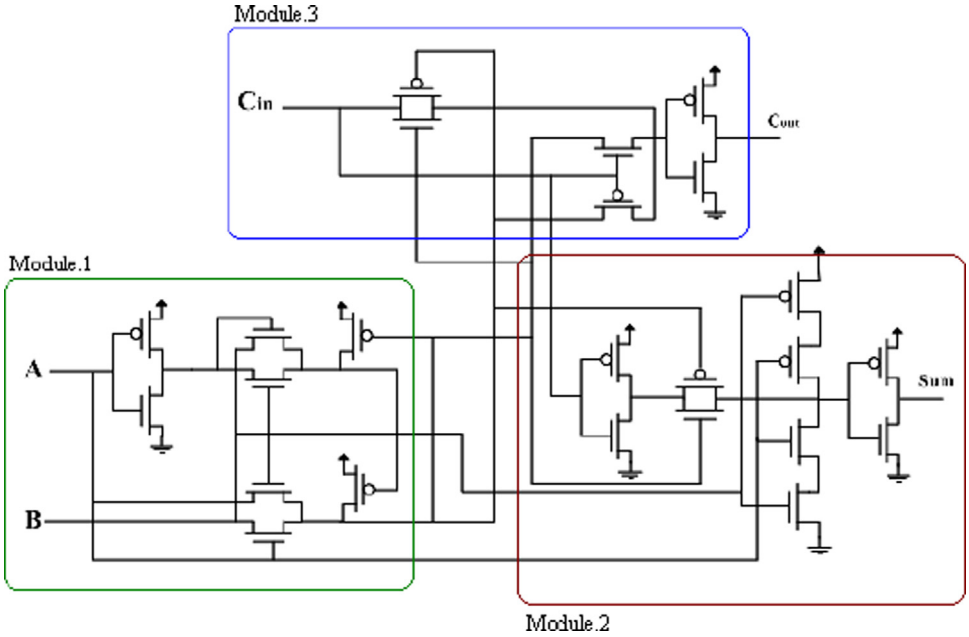

Fig. 1. Hybrid-CMOS full adder.