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Compact thermal modeling for packaged microprocessor design with practical power maps ☆

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ABSTRACT

In this paper, we propose a new behavioral thermal modeling technique for high-performance microprocessors at package level. Firstly, the new approach applies the subspace identification method with the consideration of practical power maps with correlated power signals. We show that the input power signal needs to meet an independence requirement to ensure the model predictability and propose an iterative process to build the models with given error bounds. Secondly, we show that thermal systems fundamentally are nonlinear and then propose a piecewise linear (PWL) scheme to deal with nonlinear effects. The experimental results validated the proposed method on a realistic packaged integrated system modeled by the multi-domain/physics commercial tool, COMSOL. The new piecewise linear models can model thermal behaviors over wide temperature ranges or over different thermal boundary convective conditions due to different fan speeds. Further, the PWL modeling technique can lead to much smaller model order without accuracy loss, which translates to significant savings in both the simulation time and the time required to identify the reduced models compared to the simple modeling method by using the high order models.

1. Introduction

Temperature has become a major concern for high performance microprocessor and package design as more devices are integrated on a chip [3,4]. Thermal management and related design problems continue to be identified by the Semiconductor Industries Association Roadmap [5] as one of the five key challenges during the next decade to achieve the projected performance goals of the industry. Thus, accurate and efficient thermal modeling and analysis is vital for the thermal-aware chip and package designs to improve performance, reliability, as well as for efficient online temperature regulation and management [6–8].

The traditional bottom-up approaches including FEM (finite element), FDM (finite difference), and computational flow dynamics (CFD) based methods were widely used for thermal modeling and analysis in the past [9–11]. For compact modeling, many existing approaches try to use thermal resistors and capacitors with fixed topology networks subject to different thermal boundary conditions [12–14]. However, the accurate RC values of elements, especially for complex geometries and boundary conditions, are difficult to determine, and the calibration against the numerical field solvers or analytical results [15,16] and measured data are usually required [17].

For thermal modeling at the architecture or package levels, many works have been proposed targeting at different applications at different abstract levels in the past. An excellent survey on recent works can be found in [18]. In general, existing approaches can be classified into bottom-up white-box approaches, which are based on the thermal dynamic physics and approximation techniques, the top-down black-box behavioral modeling approaches and the third modeling approaches, which are something in between the two approaches [18].

Existing work on HotSpot [19,8] attempts to solve this problem by generating the compact thermal model in a bottom-up manner based on processor and package structures. However, such white-box models may suffer from accuracy issues for complicated structures and boundary conditions, which are not properly modeled in the starting models. For instance, complicated package design may require exploration of packages with different structures and materials and boundary conditions for their thermal performance in the industry setting.

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Recently, top-down black-box behavioral thermal modeling methods have been proposed. Many proposed models target at the on-line temperature regulation applications, in which compact thermal models can estimate or predict the thermal behaviors of a real systems and they can be built in a dynamic way based on the online thermal sensor reading and online power estimation techniques [20–22]. Recently a distributed online thermal model was proposed and validated on a realistic many-core system [23–25].

Another important development for the top-down black-box thermal modeling is for building more accurate and even parameterized thermal models for architecture or package level thermal-aware design and optimization. The input power signal and output thermal temperatures for learning or training are assumed to be measured from off-line complicated equipments in the lab. Existing works consist of the matrix pencil method [26] and the subspace identification method [27,1,2]. The major advantage of such pure behavioral modeling methods is their flexibility and easy to use as no physical restrictions and assumptions are made or required for the models. They are also very accurate as the training is based on measured data. However stability and other model properties of thermal systems need to be enforced explicitly.

Recently, Beneventi et al. [18] proposed a hybrid (or *gray-box*) identification method, in which a pre-structured compact model under physical constraints is built via an optimization approach. The main advantage of such models is that many physical properties such as stability and passivity can be satisfied automatically. But such models will be less flexible for different architectures and structures as the thermal models or topologies are based on specific architectures. Also, all the existing thermal behavioral modeling methods assume that the thermal systems are linear, which may not be the case for many practical thermal systems as we show in this work, and they have difficulty to deal with varying thermal boundary conditions.

In this work, we still focus on the black-box based thermal modeling scheme based on the subspace identification method. We consider practical measured power maps, which can be obtained from thermal lab based on the test thermal vehicle (testing thermal chips). We first observe that the subspace identification method may suffer from the lack of predictability problems in general [28,29], especially when the input power is given as series of 2-dimensional power distributions (called *power maps*) in which the input signal is highly spatially correlated. Power map-based thermal characterization is widely used in industry for thermal characterizations of package design as power maps can be easily obtained (measured or computed) practically. However, the spatially correlated power signals in the power map make the system identification process more difficult. The reason is that it is difficult to distinguish the contribution from specific input when all the inputs have the same or similar transient waveforms. Also compact behavioral thermal modeling for changing boundary conditions still remain to be a challenging problem.

In this paper, we present a new behavioral thermal modeling technique considering more practical power maps and nonlinear effects of thermal systems for package level design space exploration of high-performance microprocessors. The new approach consists of two major contributions or improvements over existing approaches:

- First, we observe that the subspace identification method may suffer predictability problem when power maps are given where power inputs are spatially correlated. For instance, the busy ALU will be likely to have frequent memory accesses and many instruction fetching activities. As a result, the corresponding function units will have power increases or decreases at the same or similar times. Such correlated input signals pose difficulty for the subspace identification method and will easily lead to loss of predictability as it is more difficult to distinguish the contributions from specific inputs when all the inputs have the same or similar transient waveforms. In this paper, we show that the input power signal needs to meet some independence requirements to ensure model predictability (rank of input power maps or their power signal matrix needs to meet certain requirements). A new algorithm, *ThermSubCP*, can generate independent power maps to meet the spatial rank requirement and can also automatically select the order of the resulting thermal models for the given error bounds.
- Second, we show that thermal systems are fundamentally nonlinear. One important example is that thermal conductivities of silicon and package materials are temperature dependent. Another example is the changing thermal boundary conditions due to different fan speeds. To mitigate this problem, we apply the piecewise linear (PWL) scheme to characterize the nonlinear thermal behavior under those conditions. Our experiments show that the nonlinear effects in the thermal systems are typically mild and weak but are still significant enough to warrant the PWL modeling. However, nonlinearity due to boundary conditions can be very significant. PWL can deal with both mild and hard nonlinearities. We observe that the PWL method can lead to smaller models and reduced modeling costs compared to high order model approximation. This is important as the costs of identifying and simulating the reduced models will grow at least quadratically, it is critical to reduce the model order to maintain the efficiency gain from the reduced order modeling. The new modeling algorithm, *ThermSubPWL*, partitions the nonlinear ranges (due to temperature or boundary condition changes) into a number of small ranges and performs the modeling on each range using the previously proposed *ThermSubCP* method. A linear transformation method, which avoids the existing multi-transition requirement, is proposed to transform the identified linear local-models to the common state basis to build the continuous piecewise linear model. To the best knowledge of the authors, the proposed method is the first work addressing the nonlinear thermal modeling problem.

Experimental results validate the proposed method on a realistic packaged integrated system modeled by the multi-domain/physics commercial tool, COMSOL, under practical power signal inputs. The new piecewise linear models can model thermal behavioral over wide temperature ranges and different thermal boundary convective conditions due to different fan speeds. Further, the PWL modeling technique can lead to much smaller model order without accuracy loss, which translates to significant simulation time reduction and about 10 × less time to identify the reduced models compared to the simple modeling method by using the high order models in our examples.

The rest of this paper is organized as follows: Section 2 presents the thermal modeling problem we are trying to solve. Section 3 reviews the subspace identification method. Section 4 presents the new power-map based thermal modeling technique, and Section 5 gives the new nonlinear thermal modeling technique. Finally, Section 6 presents the experimental results of both *ThermSubCP* and *ThermSubPWL*, with Section 7 concluding the paper.

2. Thermal modeling problem considering power maps

We first present how the power inputs are modeled in our problem. A microprocessor chip is partitioned into $p = n \times m$ power grids as shown in Fig. 1, where each square power grid has a power source as an input and the measured temperatures at