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High power density AlGaAs/InGaAs/GaAs PHEMTs using an optimised manufacturing process for Ka-band applications

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ABSTRACT

In this study, a novel manufacturing process for a 0.1 μm T-gate is investigated for producing a high output power performance for the Ka-band frequencies using high-quality AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistors (PHEMTs) on semi-insulated (SI) GaAs substrates. The gate manufacturing process is the most important process due to its intimate relationship with the DC and RF performance of the device. To improve the gate performances of PHEMT devices, we investigated various materials and processing approaches involving a wide gate recess, double exposure by e-beam lithography, and low-damage double-gate passivation methods based on plasma-enhanced chemical vapour deposition (PECVD). To reduce the sensitivity to current collapse effects, we investigate the relationship between the electrical characteristics of the PHEMTs and top and bottom gate-supported passivation films. To improve the ohmic contact performance, we test an AuGe/Ni/Au (200/30/120 nm) ohmic contact metallisation scheme using the rapid thermal annealing (RTA) process at temperatures ranging from 450 °C 30 s. A PHEMT with a gate length of 0.1 μm, exhibiting a maximum drain current density of 680 mA/mm, a peak transconductance of 500 mS/mm, a unity-gain cut-off frequency (f_T) of 56 GHz, and a maximum frequency of oscillation (f_{MAX}) of 84 GHz, is demonstrated using this novel manufacturing process; the Ka-band power performance includes an output power density of 2.4 W/mm and a power-added efficiency (PAE) of 44.6%.

1. Introduction

Due to their excellent high-frequency operation, high efficiency, high power, and low-noise performance, AlGaAs/InGaAs/GaAs PHEMTs are emerging as promising candidates for radio frequency (RF) components, such as low-noise amplifiers or power amplifiers for the next-generation of commercial wireless communication systems [1–4]. In particular, in the case of extremely high frequencies, GaAs-based PHEMTs have attracted a great deal of interest as active components. For optimised high-frequency operation, high-quality gate fabrication, reduced parasitic gate resistance (R_g), and high power performance are the most important issues to determine the performance of PHEMTs. Low R_g can be obtained at high frequencies, and high value of f_T and f_{max} can be obtained. To reduce the gate resistance, T-shaped gates with a small gate length and large cross-sectional area are required [5–7]. T-gate fabrication can be based on electron beam lithography with multiple resist layers [8,9]. The gate length (L_g), and the thickness of the passivation layer are the major factors affecting the gate capacitance (C_{gs}), which is a key parameter in determining the RF performance in the high-frequency range. The T-gate head is a function of the reduction of R_g. However, at the same time, the T-gate head is a function of the increase in C_{gs} [10–12]. Likewise, to increase the output power, the high drain current density, high breakdown voltage, and knee voltage are required. These relationships can be shown in a simple equation:

$$P_{out} = \frac{I_{DS,max}(V_{break} - V_{knee})}{8} \quad (1)$$

where $I_{DS,max}$ is the maximum drain current from DC measurements and V_{break} and V_{knee} are the breakdown and knee voltages, respectively [13]. To obtain high power, there are three key parameters, as shown in Eq. (1): a high drain current density, high breakdown voltage, and low knee voltage. In spite of its high-frequency performance, unfortunately, GaAs PHEMTs have a high drain current density and a high breakdown voltage performance compared with GaN HEMT structures due to the different epi material characteristics and structures. Moreover, the large gate leakage current and current dispersion that are generated due to the surface states remain the most significant obstacles to high-frequency operation in AlGaAs/InGaAs/GaAs PHEMTs. It is noted that the current collapse condition can be considerably improved by surface passivation methods [14].

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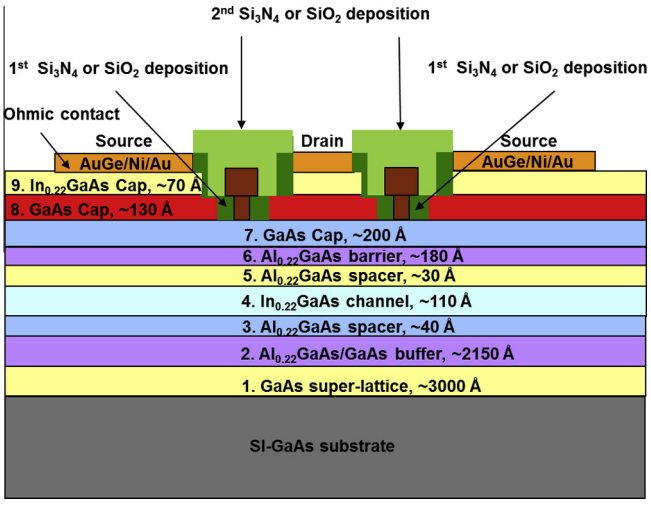

Fig. 1. A cross-sectional schematic diagram of an AlGaAs/InGaAs/GaAs PHEMT.

To increase output power using the GaAs epi structure, in this work, we employed a SI-GaAs substrate-based AlGaAs/InGaAs/GaAs PHEMT fabrication process, which is highly competitive in terms of the device performance and cost. To improve the device characteristics, several optimised processes are presented. First, an optimised AlGaAs/InGaAs/GaAs epi-structure using a changeable AlGaAs barrier thickness and Al composition is proposed [15]. Second, to mitigate the current collapse problem and increase C_{gs}, a double-gate-supported passivation scheme (Si_3N_4/Si_3N_4; SiO_2/SiO_2; SiO_2/Si_3N_4; Si_3N_4/SiO_2) is first proposed for AlGaAs/InGaAs/GaAs PHEMTs [16]. In addition, a damage-free dry/wet-etching method is proposed that removes the undesirable passivation layers. Passivation films provide effective improvements that mitigate the current collapse phenomenon. However, the suppression of the current collapse phenomenon in high-frequency and high-power operations cannot be achieved using only the passivation process. An advanced 0.1 μm gate manufacturing process with a double-exposure method using electron beam lithography and a wide gate recess process increases the drain-to-source breakdown voltage, and more stable operation can be achieved in the high-frequency range.

2. Experimental procedure

AlGaAs/InGaAs/GaAs-structured epitaxy materials are grown by metal organic chemical vapour deposition (MOCVD) on a 6-in. SI-GaAs substrate, which consists of the following layers: a 3000 Å GaAs, 2150 Å $Al_{0.22}GaAs$/GaAs buffer, silicon delta first doping of 1.5×10^{12} cm^{-2}, 40 Å $Al_{0.22}GaAs$ spacer, 110 Å $In_{0.22}GaAs$ channel, 30 Å $Al_{0.22}GaAs$ spacer, silicon delta second doping of 5×10^{12} cm^{-2}, 180 Å $Al_{0.22}GaAs$ barrier, 230 Å GaAs cap layer, silicon delta final doping of 6×10^{12} cm^{-2}, and 70 Å $In_{0.22}GaAs$ cap layer. The proposed process starts with mesa isolation, after which the AuGe/Ni/Au (200/30/120 nm) source and drain ohmic metal is deposited by an e-beam evaporator. After the ohmic metal lift-off process, the samples are sequentially annealed under an N_2 flow using the rapid thermal annealing (RTA) process at temperatures ranging from 450 °C 30 s. After the RTA processing, the specific contact resistances (ρ_c) are measured by the transfer length method (TLM); the square (100×100 μm) contacts are separated by 2, 4, 8, 16, and 32 μm. The circular TLM data indicated a ρ_c of below 10^{-5} Ohm cm^2 with a sheet resistance of approximately 400 Ohm/sq. After ohmic processing, wide double-recessed etching is conducted. A gate recess surface passivation layer composed of Si_3N_4 or SiO_2 is then deposited by PECVD to a thickness of 100 nm. After the deposition of Si_3N_4 or SiO_2, a 0.1 μm gate foot pattern is realised by double-exposed e-beam lithography. After the developing process, inductively coupled plasma (ICP) dry etching is performed to selectively remove the Si_3N_4 or SiO_2. After that, a Ni/Au (40/400 nm) T-gate with a length of 0.1 μm was formed between the source and drain ohmic contacts. The passivation process was performed after all of the aforementioned steps, followed by the formation of vias to open the metal contacts. A cross-sectional schematic diagram of an AlGaAs/InGaAs/GaAs PHEMT on a SI-GaAs substrate is shown in Fig. 1.

2.1. Wide gate double recess process method

Due to the creation of a depletion region, the flow of current from source to drain is blocked and, eventually, only a small amount of current flows compared with the supplied voltage. This implies that the breakdown voltage of the device is not good, which can be solved by the wide double-recessed process [17]. Through the use of a wide recess with gate recess, the area of the channel covered by external air can be decreased by establishing

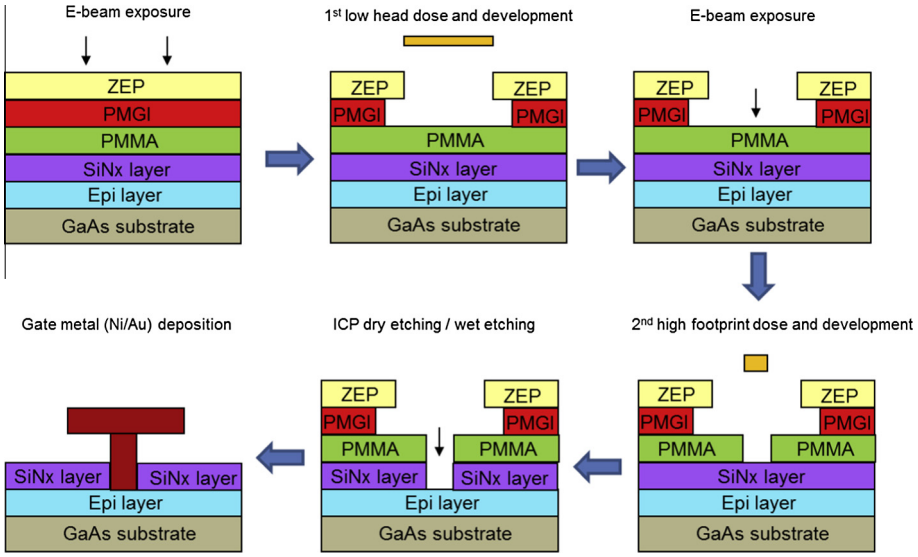

Fig. 2. Flow chart of the double-exposure e-beam lithography method.