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Statistical full-chip total power estimation considering spatially correlated process variations ☆

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ABSTRACT

In this paper, we propose an efficient statistical full-chip total power estimation method considering process variations with spatial correlation. Traditionally, dynamic power and leakage power were computed separately as leakage power is more susceptible to process variations. But in the end, it is total power that designers will be concerned with. We propose a new method to compute the statistical total power via circuit level simulation under realistic input testing vectors. To consider the process variations with spatial correlation, we first apply principle factor analysis method (PFA) or its weighted version (wPFA) to transform the correlated variables into uncorrelated ones and meanwhile reduce the number of resulting random variables. Afterwards, Hermite orthogonal polynomials and sparse grid techniques are used to estimate total power distribution in a sampling way. The proposed method has no restrictions on models of statistical distributions for total powers. The method works well when strong spatial correlation exists among random variables in the chip. Experimental results show that the proposed method has 100*X* times speedup than the Monte Carlo method under fixed input vector and 20*X* times speedup than the Monte Carlo method considering both random input vectors and process variations with spatial correlation.

1. Introduction

As power has become a limited factor for many nanometer VLSI systems, accurate estimation of full-chip total power is crucial for design optimization and sign off. For digital CMOS circuits, the total power consumption is given by the following formula:

$$P_{total} = P_{dyn} + P_{short} + P_{leakage}, \quad (1)$$

in which P_{dyn}, P_{short} and $P_{leakage}$ represent dynamic power, short-circuit power and leakage power, respectively. Most of the previous works on power estimation either focus on dynamic power estimation or leakage power estimation.

Early research on power analysis is mainly focusing on dynamic power analysis considering random input patterns. Monte Carlo based simulation was proposed in [2–4] where the circuit is simulated for a large number of input vectors to gain statistics for average power. Later, probabilistic methods for power estimation were proposed and widely used [5–9] because statistical estimation can be obtained without time-consuming exhaustive simulation. In [5], the concept of probability waveforms is proposed to estimate the mean and variance of the current drawn by each circuit node. In [6], the notion of transition density is introduced and they are propagated through combinational logic modules without regard to their structure. However, the author did not consider the inner signal correlation, thus the algorithm is only applicable to combinational circuits. Ghosh et al. [7] extended the transition density theory to consider sequential circuits via the symbolic simulation to calculate the correlations between internal lines due to reconvergence. However, the performance of this algorithm is restricted due to its memory space complexity. In [8,9], the authors used the tagged probabilistic simulation (TPS) to model the set of all possible events at the output of each circuit node. The method is more efficient compared with [7] due to its effectiveness in computing the signal correlation.

Later on, as technology scales down to nanometer ranges, the process induced variability has huge impacts on the circuit

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performance [10]. Designers realize that leakage power is becoming more and more significant and is very sensitive to the process variations. Further more, many variational parameters in the practical chips in nanometer range are spatially correlated, which makes the computations even more difficult [11]. Simple assumption of independence for involved random variables can lead to significant errors. As a result, full chip leakage power estimation considering process variations under spatial correlation has been intensively studied in the past [12–17], the method can be grid based [13,14,17], analytical expression based [12], projection based [15], simplified gate leakage model based [16].

On the other hand, even if leakage power could contribute significantly to the total power consumption in low power design, dynamic power usually accounts for the major potion in the total power for a reasonably designed circuit [18]. Recently, researchers began to realize the significant impact of process variation effect on dynamic power and several research works have been proposed. Harish et al. [19] used hybrid power model based on Monte Carlo analysis, but the method is only applied to a small two-stage 2-input NAND gate. Pilli et al. [20] presented another approach, which divides the clock cycle into a number of time slots and the transition density is computed for each slot, but only mean value of dynamic power can be estimated. The work in [21] used a variation delay model to obtain minimum and maximum delay bound in order to estimate the number of glitches and dynamic power. In [22], the authors used supergate and timed Boolean functions to filter glitches and consider signal correlations due to re-convergent fanouts. The work in [23] introduced a new method based on *transition waveform* concept, where transition waveform is propagated through the circuit and the effect of partial swing could be considered. However, none of these listing works considered the process induced variations with spatial correlation which has already been intensively studied for leakage power estimation.

Although total power can be computed by simply adding the dynamic power and leakage power (plus short-circuit power), practically, dynamic power and leakage power are correlated. For instance, leakage power of a gate depends on its input state, which depends on the primary inputs and timing of the circuits. Using dominant state or average values is less accurate than the precise circuit-level simulation under realistic input vectors. Under the process variations with spatial correlation, the dynamic power and leakage power are more correlated via process parameters. As a result, traditional separate approaches will not be accurate. Circuit level total power estimation based on real testing vectors is more desirable.

Fig. 1 shows the comparison of the circuit total power distribution of c432 from ISCAS'85 benchmark. We show two power variations. The first figure (upper) is obtained due to random input vectors. The second is obtained using a fixed input vector but under process variations with spatial correlation. As can be seen that, the variance induced by process variations is comparable with the variance induced by random input vectors. As a result, the effect of process variations with spatial correlation cannot be neglected during total power evaluation.

In this paper, we propose an efficient statistical chip-level total power estimation (STEP) method considering process variations under spatial correlation in which both the dynamic power and leakage power are included. To the best knowledge of the authors, it is first work toward the statistical total power analysis. The new method use the commercial Fast-SPICE tool to obtain total chip power. To consider the process variations with spatial correlation, we first apply principle factor analysis method (PFA) or its weighted version (wPFA) to transform the correlated variables into uncorrelated ones and meanwhile reduce the number of resulting random variables. Afterwards, Hermite polynomials and sparse grid techniques are used to estimate total power distribution in a sampling way. Experimental results show that the proposed method is 100*X* times faster than the Monte Carlo method under fixed input vector and 20*X* times faster than the Monte Carlo method considering both random input vectors and process variations with spatial correlation.

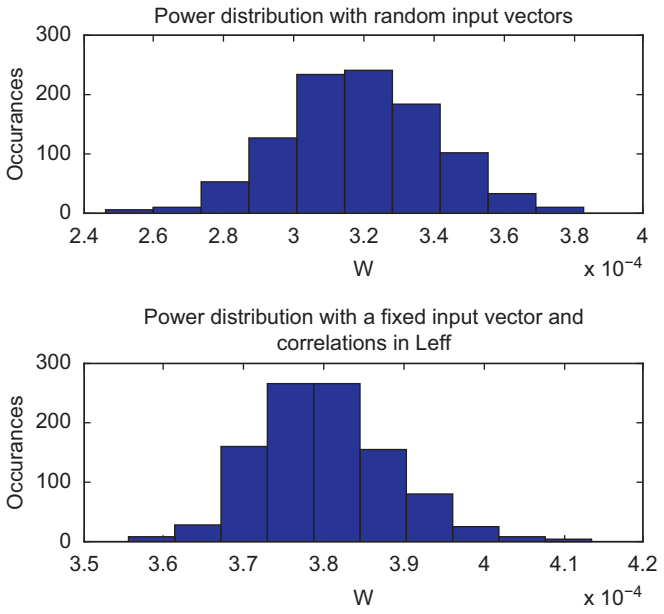

Fig. 1. The comparison of circuit total power distribution of circuit c432 in ISCAS'85 benchmark sets (top) under random input vectors (with 0.5 input signal and transition probabilities) and (bottom) under a fixed input vector with effective channel length spatial correlations.

The rest of the paper is organized as follows: In Section 2 we review the Monte Carlo based power estimation method. Section 3 describes the proposed method of total power estimation under process variations with spatial correlation. The experimental results are presented in Section 4 to validate our method. Finally, Section 5 concludes this paper.

2. Review on the Monte Carlo-based power estimation method

In general, dynamic power P_{dyn} is expressed as follows:

$$P_{dyn} = \frac{1}{2} f_{clk} V_{dd}^2 \sum_{i=1}^{n} C_i S_i, \tag{2}$$

where n is the number of gates on a chip, f_{clk} is clock frequency, V_{dd} is the supply voltage, C_i is the sum of load capacitance and equivalent short-circuit capacitance at node i, and S_i is the switching activity for gate i. Many previous works about dynamic power estimation are based on (2), they can be Monte Carlo based [2–4] or probabilistic based [6,9]. The Monte Carlo based method is considered more accurate than probabilistic based method and at the same time without losing much efficiency [2]. In the Monte Carlo based method, the switching activity S_i in (2) can be modeled as

$$S_i = \frac{n_i(T)}{T}, \tag{3}$$

in which $n_i(T)$ is the number of transitions of node i in the time interval $(-T/2, T/2]$. The mean power P_T is defined as:

$$P_T = E[P_{dyn}]. \tag{4}$$