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32 nm node BEOL integration with an extreme low-*k* porous SiOCH dielectric *k* = 2.3

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ABSTRACT

A 32 nm node BEOL integration scheme is presented with 100 nm metal pitch at local and intermediate levels and 50 nm via size through a M1-Via1-M2 via chain demonstrator. To meet the 32 nm RC performance specifications, extreme low-*k* (ELK) porous SiOCH *k* = 2.3 is introduced at line and via level using a Trench First Hard Mask dual damascene architecture. Parametrical results show functional via chains and good line resistance. Integration validation of ELK porous SiOCH *k* = 2.3 is investigated using a multi-level metallization test vehicle in a 45 nm mature generation.

1. Introduction

A key point for BEOL interconnects at each new node is the reduction of RC delay. Nevertheless, for each generation, line resistance drastically increases due to both line section reduction and copper resistivity raise [1]. Thereby, capacitance reduction is the solution to maintain steady RC delay. Consequently, low-*k* (LK) and ultra low-*k* (ULK) are introduced: *k* = 3.0 for 65 nm and *k* = 2.5 for 45 nm [2]. For the 32 nm technology node, extreme low-*k* (ELK) porous SiOCH *k* = 2.3 dielectric with higher porosity range is developed to meet ITRS specifications [3] but faces integration issues linked to BEOL architecture scalability. In this paper, ELK material compatibility with current 45 nm Trench First Hard Mask (TFHM) architecture is evaluated [4]. Then ELK and TFHM extendibility to 32 nm technology node is determined through the first realization of single and dual damascene structures at 32 nm CMOS design rules.

2. Process integration

2.1. ELK process achievements and properties

Porous SiOCH dielectric materials (*k* = 2.5 and *k* = 2.3) are obtained by mixing a porogen material inside a SiOCH matrix. Two steps are necessary to realize these dielectrics. Firstly, the co-deposition of two precursors by PECVD is made to achieve a SiOCH skeleton containing organic species (porogen). Then, the porogen removal treatment is performed using an UV assisted thermal cure at 400 °C (Fig. 1) [5]. In order to maintain an ELK material *k* = 2.3 compatible with a multi-level metallization (MLM) process, a compromise has been obtained between the pore density and the mechanical properties of the skeleton (Table 1).

The integration in BEOL interconnects of such dielectric films are evaluated using a TFHM architecture. Among the evaluated criteria, we have studied:

- The interaction between the ELK and the metallic barrier.
- Two CMP strategies: CMP stopped on ULK (direct CMP approach) versus CMP stopped on dense capping layer (cap-layer approach).

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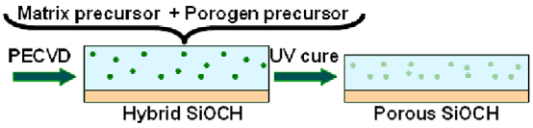

Fig. 1. Dielectric process achievement scheme.

Table 1
Materials properties of $k = 2.5$ and $k = 2.3$ dielectrics.

	$k = 2.5$	$k = 2.3$
k@100 kHz	2.5	2.3
B_v (MV/cm)	6.0	5.9
RI@632.8 nm	1.341	1.323
$E_{reduced}$ (GPa)	6	3.5
Hardness (GPa)	1	0.7
Stress (MPa)	52	37
Porosity	26%	30%
Pore radius (nm)	1.2	1.2

2.2. BEOL interconnect architecture: Trench First Hard Mask

The Trench First Hard Mask (TFHM) architecture strategy presented in Fig. 2 has already proved its robustness for the integration of ULK ($k = 2.9$) at the 65 nm and porous ULK ($k = 2.5$) at the 45 nm nodes [4].

The Hard Mask architecture is used to avoid direct contact between ULK and the resist. This architecture minimizes ULK dielectric exposition to stripping plasmas and atmospheric contamination. This integration scheme allows the change of ULK material with minimum patterning modification and consequently displays a good extendibility to lower k-value materials. The ULK patterning is followed by conventional metallic barrier (TaN/Ta barrier), seed layer, copper electroplating (ECD) and chemical–mechanical polish (CMP).

Such BEOL architecture is used to realize single and dual damascene structures with 32 nm CMOS design rules.

3. Results and discussion

3.1. Interaction between ELK and metallic barrier

In this first part, the impact of metallic barrier (TaN/Ta) and more particularly tantalum (Ta) diffusion into porous dielectrics is investigated thanks to RBS analysis on fullsheet wafers. In order to take into account the TFHM architecture patterning steps, fullsheet wafers with appropriate stack (Fig. 3) are performed. It means that same treatments (etching plasma and wet clean) used during TFHM architecture patterning are realized before metallic barrier deposition (TaN/Ta). Finally, RBS analysis is used to measure the diffusion of tantalum into porous SiOCH dielectrics $k = 2.3$ and $k = 2.5$ and dense SiOCH dielectric $k = 3$ (Fig. 4).

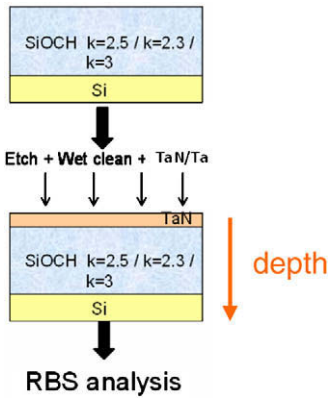

Fig. 3. Appropriate stack in order to study the diffusion of tantalum (Ta) on porous dielectrics ($k = 2.3$ and $k = 2.5$) and dense dielectric ($k = 3$) by RBS analysis.

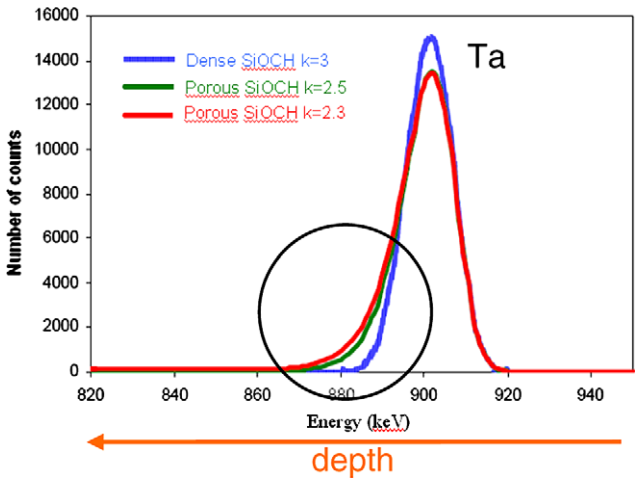

Fig. 4. RBS profile of tantalum (Ta) for porous dielectrics ($k = 2.3$ and $k = 2.5$) and dense dielectric ($k = 3$).

As expected, Fig. 4 shows that the diffusion of tantalum is more pronounced for porous SiOCH dielectrics than for dense SiOCH dielectric (black circle) and a slight difference in the Ta peak is noticed between the two porous dielectrics ($k = 2.3$ and $k = 2.5$). We can conclude that the introduction of porosity can induce tantalum penetration along the sidewall or the bottom of patterned lines.

3.2. Impact of CMP process

For the sub-65 nm generation, two CMP strategies are investigated: CMP stopped on dense capping layer (cap-layer approach, Fig. 5a) versus CMP stopped on ULK (direct CMP approach, Fig. 5b). In cap-layer approach, thickness control of the remaining cap-layer may be difficult due to metal density and CMP process

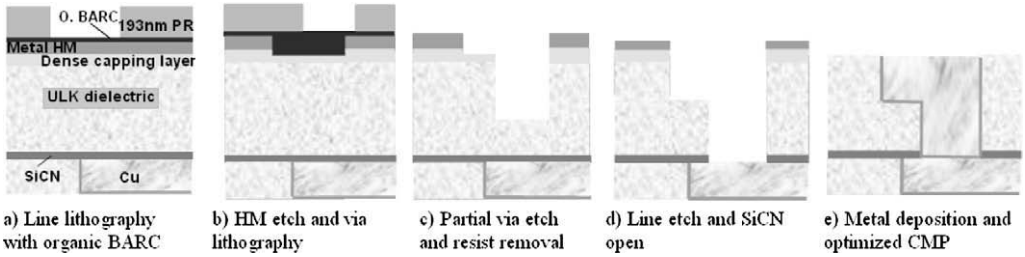

Fig. 2. Trench First Hard Mask architecture presentation.