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Analysis of electromigration induced early failures in Cu interconnects for 45 nm node

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ABSTRACT

Bi-directional current stressing was used for monitoring electromigration (EM) lifetime evolution in 45 nm node interconnects. Experimental results show that an initial bimodal distribution of lifetimes can be modified into a more robust mono-modal distribution. Since the bi-directional tests provide successive void nucleation and void healing phases, the Cu microstructure is thought to evolve once the formed void is filled thanks to EM induced matter displacement. FEM modeling is used to compare the predicted location of void nucleation for given microstructures at the cathode end: a multigrain structure is compared to a perfect bamboo microstructure. Experimental and modeling results let us assume that small grains (<linewidth or via diameter) at the cathode end present a risk of EM induced early fails. Indeed at this location void nucleates and grows nearby the via opening it shortly. On the contrary, the bamboo microstructure is thought to provide more robust lifetime because voids nucleate a few hundred nanometers in the line and grow down reaching the bottom diffusion barrier of the line. This latter case provides larger void size before circuit opening.

1. Introduction

Over the last decades, major improvements have been made in the semiconductor industry in terms of chip speed, cost, and power consumption. Such achievements have been mainly obtained with increasing device density. At the same time, the density of on-chip interconnects increases to ensure the communication between devices. This continuous downscaling of interconnect dimensions rises reliability concerns. At each new technology node, interconnects have to carry the same current but their section is reduced. The current density is hence increased needing to carefully consider interconnect reliability and in particular electromigration (EM). The latter is a mass transport driven by an electric current that can lead to formation of voids or opens in metallic wire. As a consequence it is becoming more and more difficult to meet EM robustness criteria in advanced technology nodes.

The classical approach studies EM with lifetime experiments. Simple test structures are stressed at accelerated conditions: high current density and temperature, until degradation occurs. Line failure is detected once the resistance has increased by a certain amount, typically 10%. This approach provides a significant statistic from which interconnect lifetime at operating conditions is deduced. Recently [1], detailed analysis of resistance evolution during an EM test has been shown to provide valuable information about physical mechanisms involved in void growth. In addition, quantitative results on EM related parameters, such as Cu drift velocity, or void size are available.

Usually electromigration failure statistics follow a lognormal distribution [2]. However, during process development EM lifetime distribution may present a risk of bimodal distribution introducing more complexity in the device lifetime prediction [3]. Different root causes of bimodal failure have been reported in the literature. For instance preexisting voids at via bottom in Cu-low *k* interconnect has been shown to provide early fails. The objective of this work is to provide better understanding of the mechanisms governing early failures to enhance process development learning curve.

2. Experimental

Test structures used in this study are dual damascene copper interconnects issued from the 45 nm node [4]. The stress current flows from the wide leads at the upper-level down to the test line (Fig. 1). All samples have an average line height, *h*, of 150 nm and an average line width, *w*, of 70 nm (Fig. 2) with a constant length, *L*, of 250 μm. Tests were carried out at package level at 300 °C with a stress current density of 2 MA/cm^2. During the EM stress, the electrical resistance of the copper line is measured to monitor the EM

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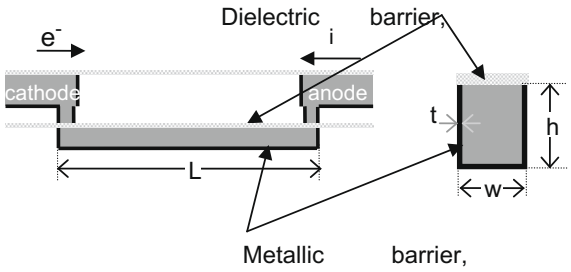

Fig. 1. Schematic diagram of the Cu interconnect test structure: (left) longitudinal view, (right) transversal view. Design values are $L = 250$ μm, $t = 8$ nm, $w = 70$ nm, $h = 150$ nm.

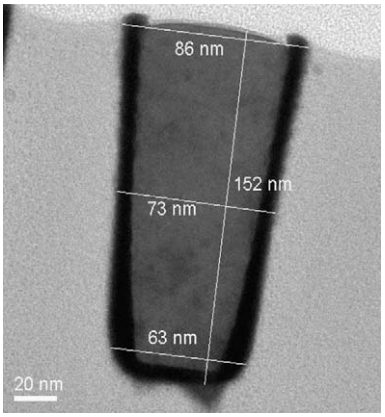

Fig. 2. TEM view of Cu line cross-section for 45 nm node.

induced damage. A 10% resistance increase criterion was used to determine the time to failure, TF. In addition, some samples were analyzed using a focused ion beam (FIB) and SEM or TEM imaging to localize and measure the EM induced voids.

In this contribution, TF follow a bimodal distribution (Fig. 3) where we have considered two failure mechanisms thanks to the details of resistance versus time curves (Fig. 4). Early fail has a resistance evolution showing a large step of resistance where the time to failure is recorded followed by a linear resistance increase. Core fail has a step of resistance with a median value of 200 Ohm similarly followed by a linear resistance increase. This last resistance trace has already been observed by other authors [5] and detailed in a previous paper [1]. Interestingly, both populations exhibit a lognormal distribution so that they can be treated as

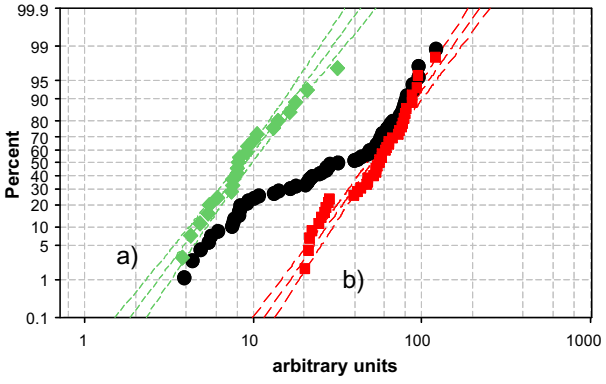

Fig. 3. Bimodal distribution of time to failure for 45 nm node, (a) early fails, (b) core fails.

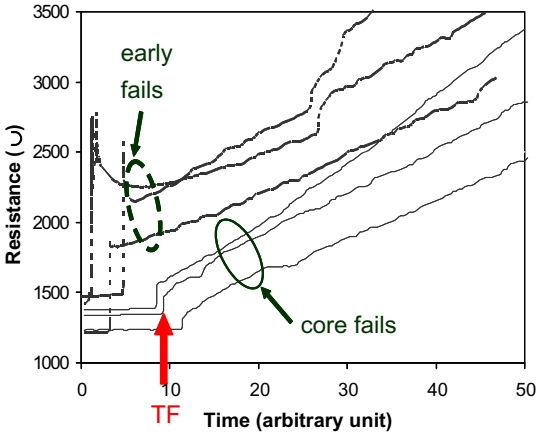

Fig. 4. Resistance traces with large step of resistance for early fails and small steps for core fails.

usual to determine electromigration parameters. TEM observation of failed devices, after 1% of resistance increase, in both early and core populations (Figs. 5a and b) shows that early fails are due to small size voids located at the line end, right beneath the via. Small void size is in qualitative agreement with a short lifetime and the large resistance step is likely due to the via opening. On the contrary, the voids of the core population are much larger and always located at some distances from the cathode via, as usually observed in mature process of previous nodes [5]. Then the step of resistance determines the void length [6].

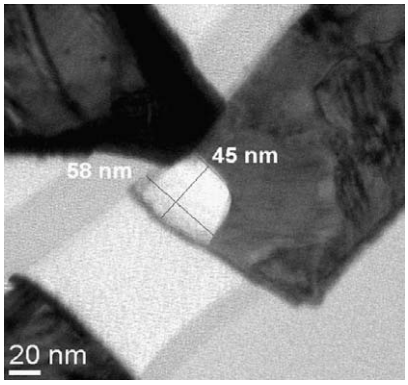

Fig. 5a. TEM at cathode side of an early fail with 1% resistance increase (electron flows from left to right).

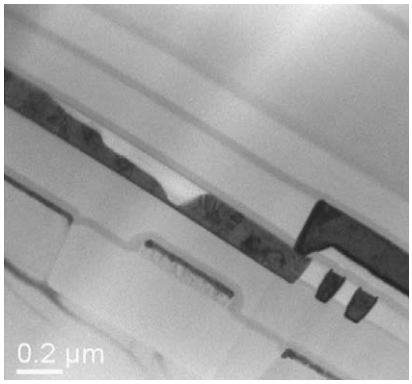

Fig. 5b. TEM at cathode side of a core fail with 1% resistance increase (electron flows from right to left).