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Strength evaluation of silicon die for 3D chip stacking packages using ABF as dielectric and barrier layer in through-silicon via

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ABSTRACT

The objective of this study is to evaluate the strength of silicon dies covered with a polymer film – Ajinomoto Build-up Film (ABF) – through the four-point bending (4PB) test and finite element method (FEM) analysis. With the evaluated strength, the possibility of die-cracking in 3D packages, wherein the thinned stacking dies are covered with ABF, under a thermal cycle condition is further investigated. In this study, a sandwich structure composed of an ABF layer as the intermediate layer between two (1 0 0) silicon substrates is applied in the 4PB test. Additionally, two kinds of bonding pressure are applied in the fabrication of 4PB specimens: 1 and 5 MPa. The force–displacement relation of the specimen is first measured by the 4PB test. On the other hand, the corresponding FEM model is simulated to obtain the relation of the first principal stress and the applied displacement. By comparing the experimental data and simulation results, the strength of the silicon substrate covered with ABF can be evaluated. Moreover, the FEM analysis results of a 10-layered die stacking 3D package show that the stress distribution in each stacking die does not exceed the evaluated strength. In summary, this paper demonstrates that the strength of the silicon substrate covered with soft and elastic material, such as ABF, as dielectric and barrier layer in 3D die stacking packages can be enhanced.

1. Introduction

As the market demands for small-sized, low-cost, high performance, and low-profile features, the electronic packaging industry has responded with the integration of a system into a single chip (System-on-Chip, SoC) or a single package (System-in-Package, SiP). Among the various kinds of advanced packages, the 3D package can provide vertical integration to achieve greater packaging density, smaller size, and better electrical characteristics by reducing the wiring length [1]. In addition to its high capability and signal transmission performance, it is also expected to ultimately become a solution for achieving the integration of multiple devices. A variety of advanced 3D stacking interconnects have been developed to meet different applications using numerous architecture for the interconnect media between each component such as package stacking, module stacking, and bare die stacking packages. Among these, the bare die stacking package is the most advanced type with regard to integration density and electrical performance. In bare die stacking packages, the majority of the wafers have to be ground relatively thin, such as 100 or 50 μm, which can cause a die-cracking problem. As such, a die crack or fracture is a common result during assembly processes or reliability tests. Die-cracking problems have been widely studied in flip chip packages with underfill [2,3]. For instance, a crack can appear in the silicon die under a thermal cycling condition. On the other hand, a crack can happen in 3D die stacking packages during a bonding process with high bonding pressure or clamping force [4].

A common bare die stacking package stacks at least two dies in a single package. Several different technologies for die stacking and signal interconnecting have been developed. Wire-bonding is a widely used interconnect method in 3D packages due to its existing infrastructure and low-cost advantages. Aside from this, other processes such as silicon side-through [5], through-silicon via (TSV) [6–8], and substrate interposer [9] have been developed. Among these, a low-cost, easily fabricated printed circuit board (PCB) processing compatible structure of a 3D bare die stack package proposed by EOL/ITRI [6,7] introduced the lamination and laser drilling process in order to form a diffusion barrier layer and a dielectric wall for the copper TSV. The Ajinomoto Build-up Film (ABF) was applied in the above process, fully covering a thinned chip for stacking at the end structure, as shown in Fig. 1. The ABF developed by Ajinomoto Fine-Techno is a most technically

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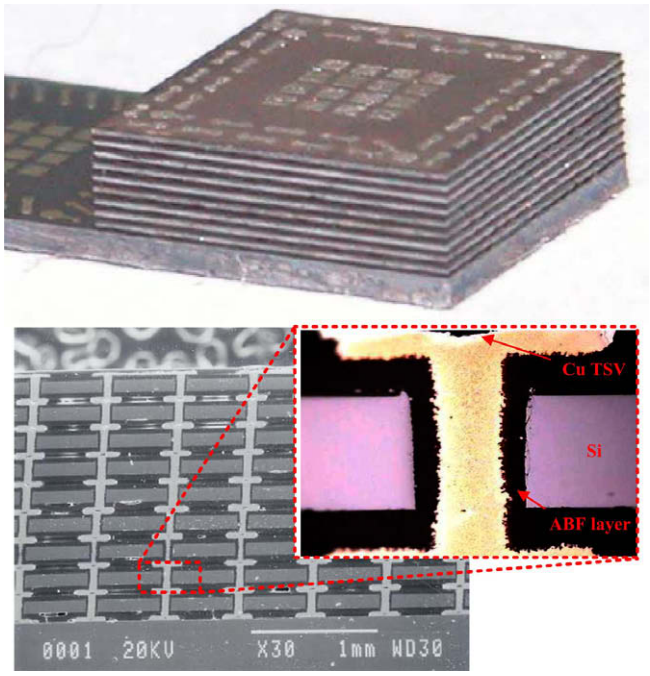


Fig. 1. 3D package structure with ABF layer [7].

advanced film-type insulation layer formation material for the print circuit board industry. The characteristic of high resin-flow property makes it suitable as insulation wall in via-filling in 3D-IC through-silicon-via proposed by ITRI. The objective of this study is to evaluate the strength of silicon dies covered with ABF using the widely accepted four-point bending (4PB) test [3,10–12] and the finite element method (FEM) analysis. With the evaluated strength, the possibility of die-cracking in 3D packages using ABF as a dielectric and barrier layer under a temperature cycling test (TCT) condition can be further investigated.

2. Analysis of the four-point bending tests

The 4PB test has been widely applied to investigate the strength of silicon dies. To determine die strength in an attempt to separate the surface grinding and edge dicing effects, the 4PB test associated with the Weibull probability analysis is employed [3]. Moreover, different test methods such as three-point bending (3PB), ball-breaker, and point-load tests have been developed for the determination of die strength [10–12]. In this study, the strength of the silicon die covered with a soft polymer film is evaluated by the 4PB test. To diminish the deformation of soft material at the loading location, a sandwich structure composed of a thin soft material layer as the intermediate layer between two (1 0 0) silicon substrates is fabricated in the 4PB test, as shown in Figs. 2 and 3. The ABF film applied in the 3D bare die package proposed by EOL/ITRI [6,7] is selected as the intermediate layer. In the specimen process, dummy 150 mm wafers approximately 650 μm thick are ground to a thickness of 500 μm on the unpolished surface. The ABF material, about 40 μm in thickness, is mechanically bonded using a pressure of 1 and 5 MPa in a vacuum environment on the polished surface of one ground wafer by the MEIKI 2-Stage Vacuum Laminator. The other wafer is then bonded on the other side of the ABF film on its polished surface. The 5 MPa pressure is the suggested bonding pressure for the ABF, while the 1 MPa pressure is applied to investigate the relation between the bonding pressure and the ultimate stress of silicon substrate. The above sandwich structure is diced into rectangular specimens with a size of

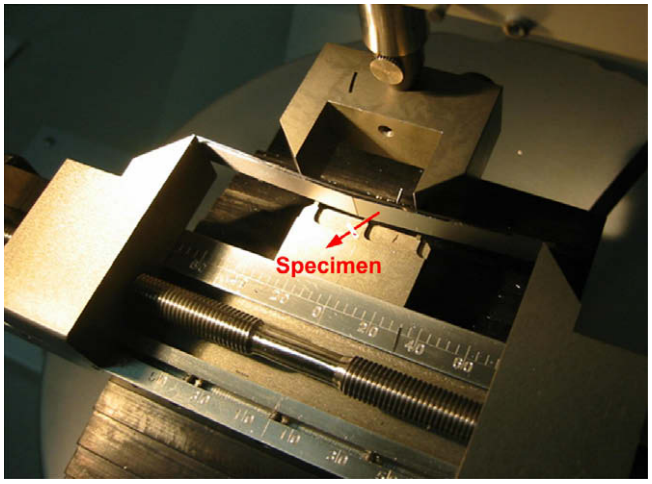
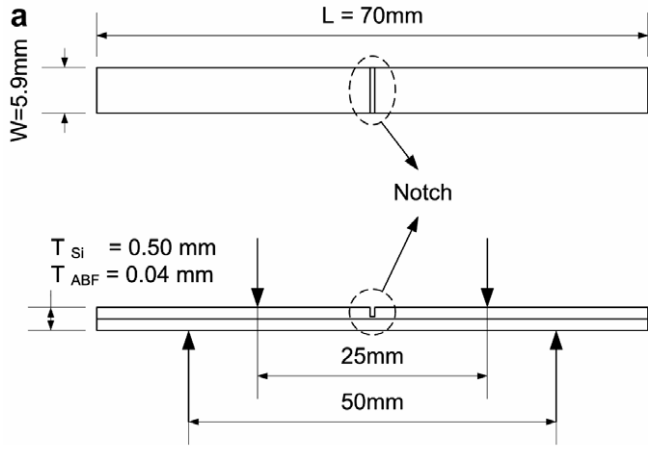


Fig. 2. Four-point bending apparatus.



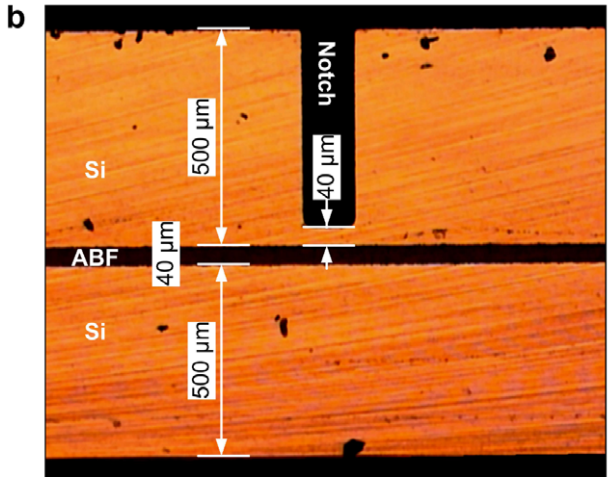


Fig. 3. (a) Schematics of the 4PB test and the geometry of specimens; (b) the optical microscope picture of the 4PB specimen around the centered notch and the detailed geometry.

70 mm (L) × 5.9 mm (W) × 1.04 mm (T), and notched at the center by a wafer-dicing machine, as shown in Fig. 3. The purpose of the notch is to ensure that the specimens will fracture at the same location under an ultimate loading condition, which can make the comparison with the FEM results more reliable. The 4PB exper-