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Source/drain extension region engineering in nanoscale double gate SOI MOSFETs: Novel design methodology for low-voltage analog applications

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Abstract

The present paper proposes for the first time, a novel design methodology based on the optimization of source/drain extension (SDE) regions to significantly improve the trade-off between intrinsic voltage gain (A_{VO}) and cut-off frequency (f_T) in nanoscale double gate (DG) devices. Our results show that an optimally designed 25 nm gate length SDE region engineered DG MOSFET operating at drain current of 10 μA/μm, exhibits up to 65% improvement in intrinsic voltage gain and 85% in cut-off frequency over devices designed with abrupt SDE regions. The influence of spacer width, lateral source/drain doping gradient and symmetric as well as asymmetrically designed SDE regions on key analog figures of merit (FOM) such as transconductance (g_m), transconductance-to-current ratio (g_m/I_{ds}), Early voltage (V_{EA}), output conductance (g_{ds}) and gate capacitances are examined in detail. The present work provides new opportunities for realizing future low-voltage/low-power analog circuits with nanoscale SDE engineered DG MOSFETs.

Keywords: Nanoscale double gate SOI MOSFET; Source/drain extension region engineering; Low-voltage/low-power analog applications; Intrinsic voltage gain; Early voltage; Transconductance-to-current ratio; Gate capacitances; Cut-off frequency

1. Introduction

In the past few years, low-power low-voltage silicon-on-insulator (SOI) MOSFET technology has emerged as a leading candidate for highly integrated mixed-mode circuits for wireless applications. However, below the 65 nm technology node, upcoming CMOS technologies face many technological challenges, the most crucial being the short-channel effects (SCEs) that tend to degrade subthreshold characteristics and increase leakage current [1–5]. Double-gate (DG) SOI MOSFETs that overcome these limitations have thus been considered as possible candidates for device scaling at the end of ITRS roadmap [1]. As DG devices are scaled down, key figure of merit (FOM) for analog applications – output conductance (g_{ds}), is degraded whereas another analog FOM – transconductance (g_m), is improved. The increase in g_m is desirable as it leads to an improvement in unity-gain frequency ($f_T = g_m/2\pi C_{gg}$), but the increase in g_{ds} severely reduces both Early voltage ($V_{EA} = I_{ds}/g_{ds}$) and intrinsic voltage gain ($A_{VO} = g_m/g_{ds}$), thus leading to a design trade-off between f_T and A_{VO}. In addition to the degradation in g_{ds} and V_{EA}, transconductance-to-current ratio (g_m/I_{ds}) also degrades due to SCEs as devices are scaled down. g_m/I_{ds} and V_{EA} are key FOM of analog performance of a technology as they indicate the efficiency of the devices to convert dc power into ac frequency and gain performance [6]. To overcome the design trade-off between A_{VO} and f_T, certain techniques such as laterally asymmetric channel (LAC) or graded-channel (GC) design [7–12] have been proposed in the literature. However, in the nanoscale regime, it will be increasingly difficult to control the dopant profile at the source end of

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the channel to enable a feasible laterally asymmetric or graded channel concept. Therefore, alternative and innovative techniques are required for improving analog performance metric of sub-50 nm MOS devices and the following questions need to be addressed in detail:

(i) How can asymmetry be introduced in carrier profile at the gate edge towards the source and drain end to enable an improvement in the analog design parameters?
(ii) How can the trade-off between cut-off frequency and intrinsic voltage gain be improved for nanoscale DG devices?
(iii) What are the optimal bias conditions and device parameters of SDE engineered MOSFETs for improved performance?
(iv) Do MOSFETs with asymmetric SDE regions perform better than those designed with symmetric SDE regions?

In the present work, we answer the above questions in detail and propose a novel method of improving the intrinsic voltage gain (A_{VO}) and cut-off frequency (f_T) of nanoscale DG devices for low-voltage/low-power analog applications. We use the concept of source/drain extension (SDE) region engineering [13–22] to significantly improve the analog FOM of nanoscale DG MOSFET. The impact of SDE region engineering is analyzed through the optimization of spacer width (s) and doping gradient (d) and the usefulness of asymmetrically designed source and drain extension regions to improve key analog parameters in nanoscale DG devices is demonstrated for the first time. Our focus for device design and optimization is in the weak and moderate inversion region, targeting applications for the low/moderate frequency, low-voltage/low-power baseband applications. The work shows new opportunities for analog applications with nanoscale DG devices.

2. Simulation

The DG devices (Fig. 1a) analyzed here have been simulated using 2D simulator, ATLAS [23]. The doping (N_a) of p-type SOI layer of 10^{15} cm^{-3}, gate workfunction of 4.72 eV, gate oxide thickness (T_{ox}) = 1.3 nm, silicon film thickness = 10 nm and gate length (L_g) = 25 nm were chosen for the devices. The spacer width (s) at the source end (s_s) and drain end (s_d) were both varied from (0.5)L_g to (2.0)L_g. The source/drain doping profile [13–15], defined by its gradient at the gate edge towards the source (Fig. 1b), was varied from 3 to 9 nm/decade. The simulations have been performed with CVT mobility model, which has shown to track the universal mobility curve [22], with default parameters. As our region of interest for operation is the weak and low-moderate inversion i.e. $V_{gs} - V_{th} \leqslant 100$ mV, where V_{gs} and V_{th} are the gate and threshold voltages, respectively, we believe that CVT model [23] is sufficient to describe the device operation.

In the present analysis, we have not considered the inversion layer quantum effect, which tends to shift the peak electron concentration away from the SiO_2 interface towards the center of the silicon film. Recent results [24] have shown that the bimodal picture of electron distribution in the silicon film as depicted by classical simulations, is still valid for film thickness down to 5 nm, thereby suggesting that quantization effects do not affect DG devices as much as single gate devices, due to volume inversion property of undoped device structure [24]. The quantum shift in threshold voltage will not be significant in undoped DG devices with $T_{si} = 10$ nm (typically less than thermal voltage ~28 mV) [25] and is therefore not considered in the analysis. The choice of $T_{si} = 10$ nm in the present work represents a well scaled device to minimize SCEs [15]. The performance of ultra-thin DG devices with $T_{si} < 10$ nm is severely limited as

(i) For $T_{si} < 5$ nm, the quantum shift in V_{th} due to finite ground state energy (inversely proportional to the square of T_{si}), becomes more difficult to control due to its high sensitivity to T_{si}.

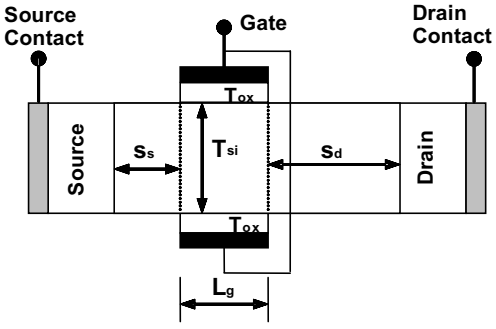

Fig. 1a. Schematic diagram of double gate SOI MOSFET simulated in the present work.

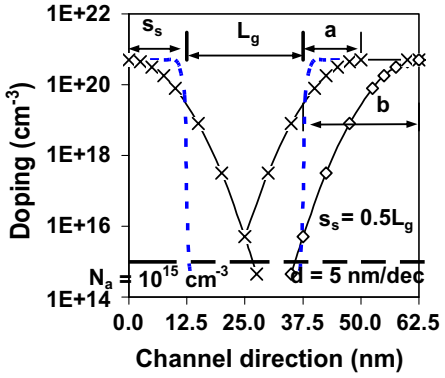

Fig. 1b. Variation of lateral source/drain doping gradient (d) along the channel at $s_s/L_g = 0.5$ for two different values of s_d/L_g (a: $s_d/L_g = 0.5$ and b: $s_d/L_g = 1$). Profiles for abrupt SDE regions (dotted line) is also shown for comparison.