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Vertical poly-Si select pn-diodes for emerging resistive non-volatile memories

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Abstract

Vertical polycrystalline silicon pn-diodes have been investigated as the select device for resistive non-volatile memories. The diodes have been fabricated up to the metal-1 level using basic processing steps of a CMOS front-end-of-line for 65 nm node and beyond. The study of the electric properties reveals that polycrystalline silicon diodes have a high current density in excess of 10^5 A/cm^2 and exhibit good rectification ratio, even at temperatures as high as 125 °C. Besides single devices, cross-point arrays with polycrystalline Silicon diodes have also been investigated.

Keywords: Vertical poly-Si diodes; Resistive RAM; Cross-point memory arrays

1. Introduction

Resistive random access memories (RRAMs) are one of the prominent candidates for the next generation of non-volatile memories (NVMs) [1,2]. Data storage in RRAMs is based on a resistance change of the memory element (see [2,3] and references therein). Regardless of the particular material used for the memory cell, RRAMs exhibit hysteretic resistive behaviour, which makes it possible to switch them between the low-resistance "1" state and high-resistance "0" state by applying current and/or voltage pulses (see [1,2,4–7] and references therein).

One of the significant advantages of RRAMs, compared to the currently available charge-storage-based floating gate NVMs, is the possibility to integrate them into the back-end-of-line (BEOL) of a standard CMOS process. In practice, this means that two consecutive metal levels in the BEOL are used as the bit- and wordlines, respectively, whereas, the memory elements are located in the adjoining vias [8]. The advantages of the BEOL integration are twofold. First, by stacking a number of memory elements on top of each other, that is, in the consecutive metal levels, the memory density can be increased without increasing the area occupied by the memory array.

Equally importantly, BEOL integration is considered particularly favorable for embedded NVMs, because it makes it possible to completely detach the front-end-of-line baseline processing from the integration of NVM on the chip.

The most compact and attractive architecture for RRAMs is the "cross-point" configuration, where memory elements are sandwiched between the word- and bitlines, offering a cell size of $4F^2$, where F is the half-pitch of the array [9]. Given that a "cross-point" RRAM is an array of resistors, it contains a large number of sneak current paths, which can cause unselected memory cells to change their original state, as well as erroneous reading. For this reason, a diode, which acts as a select device, has to be connected in series with each memory element and stacked between the word- and bitlines, as schematically shown in Fig. 1. The select diode has to sustain a sufficiently high current in the forward regime to ensure a high speed of operation, as well as to have a low series resistance com-

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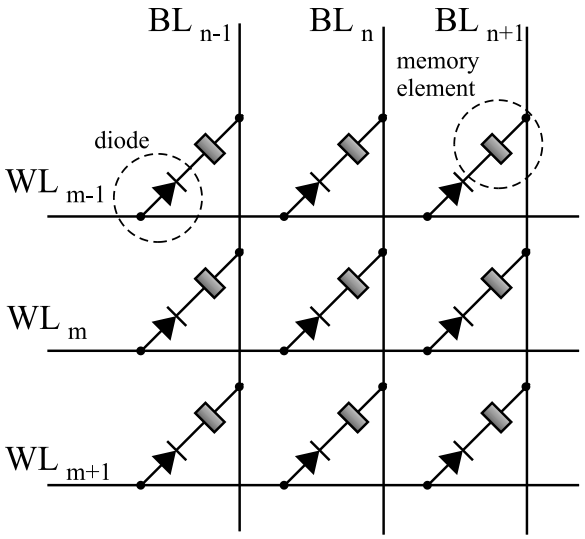

Fig. 1. A schematic of the cross-point array with select diodes and memory elements in series. WL and BL stand for the wordline and bitline, respectively. The memory elements are not the subject of this study.

pared to the memory element. Furthermore, the rectification properties of the select diode have to be good enough within the specified voltage window to prevent the writing or reading of unselected bits (disturb).

Ideally, these diodes should be manufacturable within the thermal budget of 350 °C, set by the Copper BEOL. Diodes based on non-stochiometric reactively sputtered metal-oxides had been studied for application in magnetic random access memories (MRAMs), but were abandoned due to their very low current density [9]. Metal-oxide diodes with double-barrier tunnelling have also been proposed as a candidate for the select device specifically in combination with MRAMs [10].

In this paper, we present vertical polycrystalline silicon (poly-Si) diodes intended to be used as a select device for RRAMs. Unlike in Ref. [11], where poly-Si select diodes for stand-alone anti-fuse one-time-programmable memories have been fabricated using a specifically developed in situ doped poly-Si deposition, we have chosen an approach which entirely relies on standard baseline operations, already in commercial use or set to be used for advanced CMOS nodes beyond 65 nm. Even though the quality of low temperature amorphous Silicon (α-Si) and poly-Si depositions has been significantly improved for thin film transistor applications in displays, the temperature budget, especially for the electric activation of dopants, still exceeds the limits imposed by the copper BEOL [12]. Consequently, poly-Si diodes cannot be integrated into the BEOL, but can well be embedded in a chip before the source/drain implants have been activated and silicidation has been carried out. Furthermore, poly-Si diodes can be a viable low cost option for high density stand-alone RRAMs, as they can be fabricated on an insulating substrate. Hence, the size of an RRAM array can be scaled more efficiently, since the pitch is not limited by latch-up, as is the case with vertical crystalline Si diodes [13].

2. Fabrication

The diodes were fabricated on 8″ p-type wafers. First, 150 nm of oxide was grown using wet oxidation. 100 nm of α-Si, intended for the wordlines, was then deposited with low pressure chemical vapor deposition (LPCVD), followed by a heavy boron implantation and radiation based rapid thermal anneal (RTA) at 1100 °C to ensure the complete activation and uniform distribution of boron in poly-Si. The wordlines were defined using a light-field 193 nm DUV mask and dry etching.

After the wordlines were cleaned and H-terminated with 0.3% HF to prevent the formation of native oxide, 200 nm α-Si, meant for the body of the diodes, was deposited with LPCVD and implanted with phosphorus and arsenic.

A reasonably low resistivity of poly-Si, due to the presence of the grain boundaries that act like efficient charge traps, can be achieved only if the dopant concentration exceeds 10^{18} cm^{-3} [14]. It is clear that at this scale, high diffusion constants, especially of boron, combined with high dopant concentrations pose a major challenge in fabrication of poly-Si diodes, as it is necessary to electrically activate the impurities whilst avoiding their excessive diffusion.

The thermal activation of the dopants in poly-Si diodes was carried out using ASM Levitor anneal, whose heat-conduction annealing mechanism, as opposed to the radiation of a standard RTA anneal tool, makes it possible to ramp-up the temperature at a rate of around 1000 °C/s and cool down at a rate of around 100 °C/s. As a result, the transient diffusion of boron is significantly reduced compared to RTA-anneals, where the temperatures are ramped up and down at approximately 80 °C/s. The Levitor tool has been chosen as it is likely to be used for the formation of Ni-based silicides and thermal anneal of ultra-shallow junction for the 65 nm CMOS technology node and beyond. Fig. 2 shows the spatial distribution of boron (circles), arsenic (squares) and phosphorus (triangles) in 200 nm poly-Si obtained with secondary ion mass spectroscopy (SIMS). The concentrations are normalized to the maximum concentration, which is in excess of 10^{20} cm^{-3}. The arrows indicate the positions of the junctions. In Fig. 2a boron, phosphorus and arsenic, respectively, are implanted in 200 nm of poly-Si and activated using a Levitor anneal at 1150 °C. In Fig. 2b 80 nm of poly-Si was deposited first and implanted with boron. Upon cleaning and H-terminating the poly-Si surface, 120 nm of poly-Si was deposited, implanted with phosphorus and arsenic and then subjected to 1150 °C Levitor anneal. Filled symbols show as-implanted profiles, whereas, open symbols show the spatial distributions of the dopants after the anneal. The latter approach (Fig. 2b) provides a clear advantage in terms of impurity distribution, predominantly because it helps reduce the well-known tail in the boron profile, caused by the electronic stopping. Nevertheless, due to a considerable diffusion of all impurities, the low-dose phosphorus implant, meant to define the depletion layer, has no influence on the electric characteristics of