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Layered structure in core–shell silicon nanowires

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ABSTRACT

Silicon nanowires (NWs) with core–shell structures were prepared using the Vapor–Liquid–Solid (VLS) method. The wires have lengths of several hundreds of nanometers and diameters in the range of 30–50 nm. Generally, these wires are too large to exhibit the quantum confinement effect of excitons in Si nanocrystals. However, the photoluminescence (PL) and Raman spectra are similar to those of nanocrystalline silicon embedded in a SiO_2 matrix, in which the recombination of quantum-confined excitons plays an important role. This effect occurs only when the average size of the silicon nanocrystals is smaller than 5 nm. To understand this discrepancy, TEM images of nanowires were obtained and analyzed. The results revealed that the cores of wires have a layered Si/SiO_2 structure, in which the thickness of each layer is much smaller than its diameter. The temperature dependence of the PL intensity was recorded from 11 to 300 K; the result is in good agreement with a model that takes into account the energy splitting between the excitonic singlet and triplet levels.

1. Introduction

Silicon nanostructures have attracted much attention for their capacity to serve as direct bandgap semiconductors due to the quantum confinement effect [1,2]. This characteristic enables silicon nanostructures to possess a visible emission spectrum at room temperature. Many studies have investigated porous silicon [3,4] and silicon nanocrystals embedded in a SiO_2 matrix [5,6], with the most commonly accepted argument explaining the origin of this emission being attributed to quantum-confined excitons [4]. Among various low-dimensional silicon nanostructures, silicon nanowires (Si NWs) are particularly attractive due to not only the central role of silicon to the semiconductor industry but also the potential application of this special type of nanostructure in fields of photonics, photovoltaic devices, electrical interconnects, sensors and nano-electromechanical systems. Si NWs can be synthesized by various techniques, including laser ablation [7–9], chemical vapor deposition [10,11], thermal evaporation [12–19], and solid-state growth from silicon substrates [20]. Among these methods, much attention has been paid to the thermal evaporation method due to its cost effectiveness, ease of operation, and lack of use of toxic silane gas for growing Si NWs. In this thermal growth method, the source material is vaporized and transported away from the source using a carrier gas. This transported material is then deposited onto the substrate surface with a deposited catalyst, where it condenses via the Vapor–Liquid–Solid (VLS) mechanism or a combination of the VLS and SLS (Solid–Liquid–Solid) mechanisms to form Si NWs [12–16]. The as-grown Si NWs are usually oxidized naturally, and their dimensions are significantly larger than the characteristic Bohr radius of silicon [21]. As a result, the emission peaks in the PL spectra of Si NWs are primarily ascribed to radiative defects in the silica covering the silicon core or the SiO_2/Si interfaces [22] rather than quantum confinement effects in silicon.

In this present work, we report on the fabrication of core–shell silicon nanowires using the thermal evaporation method with gold particles as a catalyst. The wire's core was proven to consist of alternating layers of amorphous silica and crystalline silicon with sizes comparable to the Bohr radius of the exciton in silicon. The temperature-dependent measurement of PL intensity from 10 to 300 K was performed and compared to that of silicon nanocrystals embedded in a silica matrix. A model was introduced to quantitatively explain this dependence, which confirmed the role of confined excitons. The photoluminescence excitation (PLE) spectra and the origin of the absorption bands are discussed.

2. Experimental

A *p*-Type Si wafer was thermally oxidized to grow a 20-nm thick SiO_2 layer, which serves as a diffusion barrier. The silicon

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wafer was then cut into two parts: one coated by a 10-nm thick Au film on top of the SiO_2 layer and another uncoated for later comparison. Each part was trimmed into smaller chips to allow the growth of silicon nanowires in subsequent steps. A mixture of silicon and carbon nanopowder with the weight ratio of 4:1 was used as the source material contained in an alumina boat. The boat was placed at the center of a conventional horizontal tube furnace. The gold-coated substrates were evenly located from the source material at a distance of 15 cm in the downstream side with respect to the flow of the argon carrier gas. Before heating, the entire furnace was purged thoroughly using a pure argon flow of 200 standard cubic centimeters per minute (sccm) for 30 min to remove the residual gas inside the furnace. The temperature of the furnace was subsequently raised up to 1200 °C at a heating rate of 10 °C per minute under a steady argon flow of 50 sccm. The system was maintained at 1200 °C for 1 h while the argon flow rate was maintained at 100 sccm. Subsequently, the furnace was cooled down to room temperature naturally.

The microstructure and morphology of the as-received Si NWs were analyzed using a Field Emission Scanning Electron Microscope (FESEM 4800 Hitachi), a Transmission Electron Microscope (TEM, JEM 1010, JEOL) and a Raman spectroscope (Micro Raman Labram 1B). The 325-nm line of a Helium–Cadmium laser was used as the excitation source for recording the PL spectra. The laser beam was focused through a quartz lens into a spot of diameter of approximately 100 μm on the sample, which was fixed onto the cold-finger of a cryostat. The excitation density was kept lower than 1 W/cm^2 to avoid effects of heating. The temperature dependence of the PL intensities was investigated at several temperatures over the range from 10 to 300 K using a closed-cycle Helium pumping system. A cooled Roper Scientific CCD combined with an Acton Research Spectrometer enabled an instant record of the spectra at any moment.

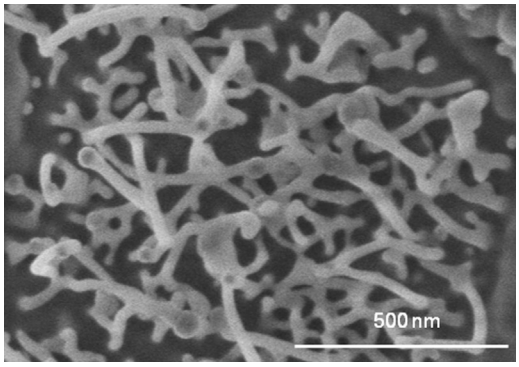

Fig. 1. FESEM image of the as-received Si NWs prepared using thermal evaporation via the VLS mechanism. Gold particles on tip of the wires can be seen clearly.

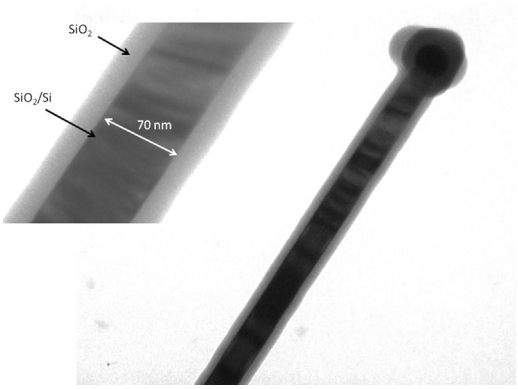

Fig. 2. TEM image of a silicon nanowire. The core–shell structure of the nanowire and layered structure of the core are visible (inset).

3. Results and discussion

The as-received silicon nanostructures can be categorized into two main types: the first type consists of those nanowires grown on gold-coated substrates via the VLS mechanism and the second type consists of those nanowires grown on uncoated substrates via the Vapor–Solid (VS) route. We obtained only amorphous SiO_2 wires on the uncoated silicon wafer, and the corresponding SEM images (not shown here) exhibited a set of worm-like wires with a diameter of approximately 120 nm. Moreover, uniform semitransparent nanowires were observed in the TEM images (not shown here), indicating that wires exhibited homogeneous structures. In the PL spectra recorded at room and low temperatures, we observed only weak blue emission bands corresponding to defect centers in the silica matrix. Fig. 1 shows the SEM image of the silicon nanowires grown on a gold-coated substrate, whose diameters range from 30 to 50 nm. Gold droplets of similar diameters were observed on tips of structures, which is a characteristic of the VLS growth mechanism. The TEM image of a particular wire reveals a core–shell structure of amorphous SiO_x–crystalline Si and thinner layers inside the core (Fig. 2). Previously, Si NWs with core–shell structures or SiO_2-sheathed crystalline Si NWs have been fabricated using the thermal evaporation method with different source materials, such as SiO [17], a Si–SiO_2 mixture [19], or a Si–carbon mixture [16]. Depending on the specific experimental conditions, the formation of a SiO_x–Si core–shell structure has been attributed to two growth mechanisms. The first mechanism involves the absorption (of SiO from vapor phase), condensation, and decomposition at the catalyst site (Au in our case, or SiO in the case that no metal catalyst is used) by the action of the catalyst according to the equation: $2SiO \rightarrow Si + SiO_2$. After decomposition, the silicon is absorbed into the catalyst island, while the oxide remains at the surface of the island. Then, Si NWs grow according to the VLS mechanisms [15,17,23]. The second mechanism involves radial oxidation with the residual oxygen in the tube furnace, resulting in the formation of an amorphous silicon oxide layer [24].

Fig. 3 shows the PL spectra excited using the 325-nm line of a HeCd laser taken at 11, 150, and 300 K. Intense red emission peaks at 685, 675, and 645 nm were observed in the spectra at 11, 150, and 300 K, respectively. It is generally accepted that the red emission bands can be attributed to the recombination of confined excitons in silicon nanocrystals [25] in the size range of ~2–5.5 nm. However, the diameter of Si NWs in our experiments has the apparent size distribution in the range of 30–50 nm, which are diameters much larger than the characteristic Bohr radius for silicon; so what is the origin of these emission bands?

To understand this discrepancy, we examined carefully the TEM image of wires shown in the inset of Fig. 2. Interestingly, we discovered that core of the wire contained alternative dark and bright strips, which can be understood as alternative layers of SiO_x and Si phases. Consequently, we propose that the core itself is an assembly of SiO_x and Si layers, where the dimensions of Si layers are comparable to the Bohr radius (5 nm). To verify the presence of the silicon crystalline phase, Raman spectra of wires were collected at room temperature. The Raman signal was rather weak because the quantity of Si NWs was very poor; however, a peak at 517 cm^{-1} can be clearly seen in Fig. 4. The appearance of this peak is evidence of the existence of silicon nanocrystals (NCs) in wires. Furthermore, the comparison of fitting the shape and position of the Raman scattering peak with the theoretical curves using the procedure described in [26] reveals that the crystalline silicon layers have an average size smaller than 5 nm, which in turn confirms the validity of our earlier proposal.