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Nano-graphoepitaxy of semiconductors for 3D integration

F. Crnogorac [a,*], D.J. Witte [a], Q. Xia [b], B. Rajendran [a], D.S. Pickard [a], Z. Liu [a], A. Mehta [a], S. Sharma [c], A. Yasseri [c], T.I. Kamins [c], S.Y. Chou [b], R.F.W. Pease [a]

[a] *Stanford University, Stanford, CA 94305, USA*
[b] *Nanostructures Laboratory, Princeton University, Princeton, NJ 08544, USA*
[c] *Quantum Science Research, Hewlett-Packard Laboratories, Palo Alto, CA 94304, USA*

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Abstract

The advantages of integrating semiconductor devices at more than one level ('3D integration') are now recognized. Key to achieving monolithic 3DICs is the ability to form single crystal semiconductor islands at the upper level without unduly heating the lower level structures. In prior work a surface relief grating of 3.8 μm pitch in the substrate was used to mediate single crystal formation while continuous wave (CW) heating a thin film of amorphous silicon; the term 'graphoepitaxy' was coined. CW heating is not possible in our case because it would overheat the lower layers. Moreover the area of the crystallites need only be about 100 nm to accommodate today's transistors. Thus we have chosen a substrate grating pitch of 190 nm (hence the term 'nano-graphoepitaxy') and a modulated CW laser to reduce the heating time to several μs. Preliminary results indicate the substrate grating lines can indeed determine the position of the crystallite boundaries when the film thickness is 100 nm; the effect is much less pronounced in 500 nm thick films.
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Keywords: Graphoepitaxy; Crystallization; Nanoimprint; Transient heating

1. Introduction

An architectural scheme involving multiple layers of active transistors stacked one above the other and connected to each other has been proposed to address the interconnect bottleneck associated with two-dimensional integrated circuits (ICs) [1]. Such three-dimensional structures have been fabricated by bonding circuits fabricated independently on Si wafers [2]. However, the vertical interconnect density of these systems has been limited to about 10^6 wires/mm^2 due to factors such as alignment limitations of wafer bonders, mismatch in the thermal expansion coefficients of different materials and particle contamination [3]. In a monolithic approach, the upper level circuits are fabricated in situ on thin single crystal films (<100 nm thick), alleviating alignment requirements and enabling much larger interconnect density. It has been demonstrated that transient heating techniques could be used to make good quality transistors on such layers without adversely affecting the quality of underlying circuits [4]. However, a practical method to obtain single crystal islands of known orientation and grain quality remains elusive. Here we describe initial work on the use of surface nano-structures and transient laser annealing as a method to achieve oriented single crystal islands of silicon over amorphous SiO_2 layers.

In prior work surface relief grating structures of 3–5 μm pitch in amorphous substrates were used to define the crystallographic orientation of deposited silicon films [5]. The melting and recrystallization of these thin films has been performed using strip-heater ovens as well as by high power continuous wave lasers. However, this mode of heat delivery is not suitable for sequential 3DIC fabrication because the long anneal time would damage devices at the lower layers. Our approach is to employ 15 μs pulses from a frequency doubled Nd:YAG laser and to use much finer structures (e.g. grating with 95 nm half-pitch) to determine the orientation of the crystal film.

* Corresponding author. Tel.: +01 650 723 0503.
E-mail address: filip@stanford.edu (F. Crnogorac).

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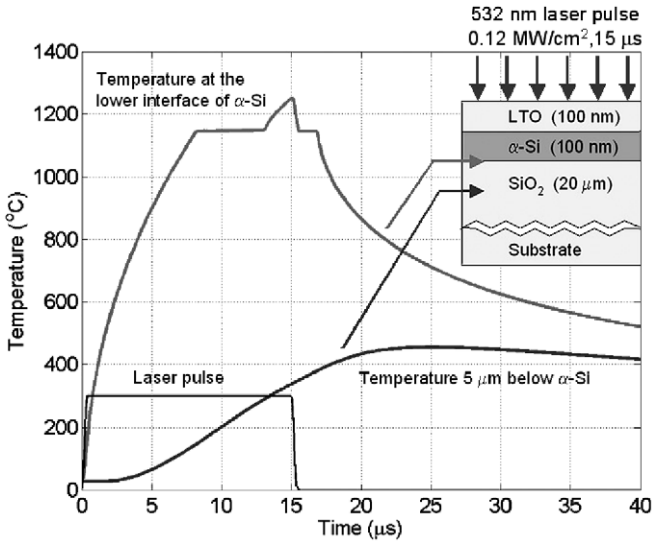

Fig. 1. One-dimensional simulation results: thermal profile evolution due to a 15 μs laser pulse anneal demonstrating complete melting of 100 nm thick α-Si layer while maintaining sub-450 °C temperature in underlying layers (5 μm below α-Si).

2. Feasibility of transient heating for 3D Integration

Drawing on a one-dimensional thermal diffusion model [4], we selected spot-size, laser power and pulse duration to ensure melting of the silicon layer while minimizing the heating of the underlying substrate [6]. The transient thermal profile for the laser-annealed wafer was obtained by solving the light absorption and heat diffusion equations for the simplified 1D structure shown in the inset of Fig. 1. Temperature dependent values of thermal conductivity, specific heat and the refractive index coefficients of the different materials were used in the calculations. We accounted for phase change by using the latent heat of fusion for the different materials. We also assumed that molten α-Si solidifies into fine-grain polysilicon with a thermal conductivity value twice that of α-Si. Random nucleation is not accounted for in the simulation and radiative losses are assumed to be negligible.

The simulation results show that by using a 15 μs laser pulse with power density of 120 KW/cm^2, the deposited amorphous silicon film (100 nm thick) could be melted completely, while keeping the maximum temperature excursion at the underlying SiO_2 layer (5 μm below) to less than 450 °C (Fig. 1). This demonstrates the feasibility of using transient heating technique to melt and recrystallize upper layers of 3D structures, without damaging circuits built in the lower layers.

3. Experimental techniques

The grating pattern was generated in thermally grown SiO_2 using nano-imprint lithography (NIL) [7]. The imprint was made in 200 nm thick thermoplastic resist with a 4 in. silicon mould using an NX-2000 machine. The imprint tool was equipped with the Air Cushion Press (ACP™) ensuring uniformity over the entire 4 in. wafer. The resulting pattern was transferred with double Cr shadow evaporation to achieve different line widths. After lift-off, the gratings were etched into thermally grown SiO_2 layer (1 μm thick) using CHF_3/O_2 reactive ion etching. Full details of the NIL procedure have been previously described elsewhere [7]. We chose different line widths from 30 nm to 70 nm, while the pitch was kept at 190 nm. Trench depth was around 25 nm and the grating profile can be seen in the atomic-force micrographs (Fig. 2). In experiments using silicon, an amorphous layer 100 nm thick was deposited at 585 °C by low pressure chemical vapour deposition (LPCVD) using silane (SiH_4) chemistry. Finally, the structure was capped with 170 nm of low temperature oxide (LTO) deposited at 400 °C. The resulting structure can be seen in the cross-sectional TEM image (Fig. 3). A second set of samples with 500 nm thick α-Si layer and 1.2 μm thick LTO cap were also fabricated. The samples were subjected to a range of laser annealing

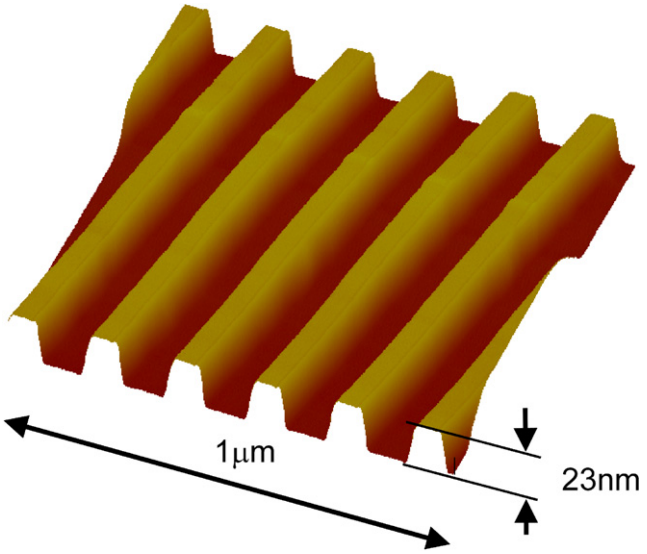

Fig. 2. AFM image and section analysis of the grating pattern etched in thermal SiO_2 using nano-imprint lithography (190 nm pitch, 70 nm linewidth).

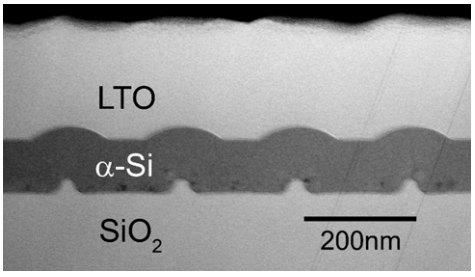

Fig. 3. TEM cross-section of the final structure: nano-imprinted grating pattern in thermal SiO_2 (190 nm pitch, 30 nm linewidth) covered with LPCVD layer of α-Si (100 nm thick) followed by a capping layer of LTO (170 nm thick).

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