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Timing analysis with compact variation-aware standard cell models

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ABSTRACT

A compact variation-aware timing model for a standard cell in a cell library is developed. The cell model incorporates variations in the input waveform and loading, process parameters, and the environment into the cell timing model. The cell model operates on full waveforms, which are modeled using principal component analysis (PCA). PCA enables the construction of a compact model of a set of waveforms impacted by variations in loading, process parameters, and the environment. Cell characterization involves describing with equations how waveforms are transformed by a cell as a function of the input waveforms, process parameters, and the environment. The models have been evaluated by calculating the delay of paths. The results demonstrate improved accuracy in comparison with table-based static timing analysis at comparable computational cost. Complexity of the models as a function of the number of parameters modeling variation is also discussed, and shows reduced memory requirements as the number of parameters describing variations increases.

1. Introduction

Circuit timing analysis is needed to ascertain if a design meets timing requirements before manufacturing. The standard approach to estimate circuit timing is through static timing analysis (STA). STA involves converting a circuit into a timing graph, where each edge represents the delay of a gate between its inputs and outputs. STA then performs a graph traversal to find the longest path, based on a project planning technique, called the Critical Path Method [1].

The delay through gates is a function of the slope of the input signals. Hence, the traditional approach to accounting for the input slope is to characterize cell delay through tables, which precompute delay and output slew as a function of input slew for each gate in a standard cell library. In order to account for slew, STA requires an additional step, a preliminary backwards traversal through the timing graph to determine the relationship between slew and delay to the output for each node in the network [2].

Circuit timing is increasingly impacted by variation due the manufacturing process and the operating environment. The standard approach to account for variation is through worst-case analysis [3]. Worst-case analysis assumes that parameters are constant within a chip, but vary between chips. Designers ensure that their design satisfies specifications for all process corners by simulating the circuit with a small set of "corner" models that represent process extremes. The "corner" models consist of tables relating delay and output slew to input slew and loading for these process extremes.

Circuit timing has, however, become increasingly susceptible to within-die variation due to both the manufacturing process and the operating environment. Hence, it has become imperative to take into account these variations in device and interconnect characteristics during design. Worst-case design does not take into account within-die variation.

To account for within-die variation, we need to perform statistical static timing analysis (SSTA) at corners that define die-to-die variation [4–12]. SSTA can determine the variation in critical path delays as a function of random and systematic variation within and between paths. SSTA resembles STA, except gates are characterized by delay distributions. The gate delay and arrival time distributions result in distributions of output delays, and correlations among these delays. Graph traversal involves applying statistical sum to arrival time distributions and the delay distribution for each gate, and statistical maximum operations to the resulting gate delay distributions.

Clearly, for SSTA we need compact models of standard cells that are accurate over parameter and environmental variations, not just at process extremes, as in worst-case design. Our proposed models can be used to generate the delay distribution functions, which can account for spatial correlations, as needed, using methods as in [6–12]. Our models can also be used directly in Monte-Carlo-based SSTA, which involves path enumeration, Monte Carlo analysis of critical paths, and the statistical maximum operation on the resulting path delays, as described in [8,13–17].

The goal of this work is to develop a methodology to construct compact variation-aware timing models for standard cells in a cell

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library, which are accurate over process and environmental variations. The model also utilizes compact models of waveforms. This paper will show that these compact waveform models, when used for static timing analysis, are more accurate than the well-known tabular method [18] and comparable in terms of computational cost.

The compact waveform models are constructed via PCA [19] of waveforms, where the waveforms are described by principal component scores (PCSs), which can reconstruct the waveforms. Moreover, since the principal component basis functions are shared among all waveforms, cell library characterization requires that we only store the equations that describe the transformations of the principal component scores as the waveform passes through the cell. The equations also describe changes in cell performance as a function of variations in the process and operating environment.

This method differs from traditional static timing analysis

(a) by working with waveforms with *realistic* shapes,
(b) by storing the waveform transformation through a cell as an *equation* rather than a table, and
(c) by including equations that describe any changes in cell performance as a function of *variations in the process and operating environment*.

This is not the first attempt to accurately model waveforms for timing analysis. Recent work has considered accurate modeling of waveform propagation through standard cells. In [20], it is shown that realistic waveforms do not resemble the idealized ramp, and in [21] it is shown that realistic waveform modeling results in more accurate timing analysis. Examples of waveform modeling include [22], where a Weibull shape parameter is added to waveform characterization to account for the differences between real waveforms and their approximation by a ramp. Other work has aimed to model realistic waveforms with a set of basis functions [23–26]. The basis functions have been selected in a variety of ways, including an error minimization heuristic, involving shifting and scaling of waveforms [23,24], PCA [25], and singular value decomposition (SVD) [26]. All prior work has shown that a few basis functions can be used to approximate realistic waveforms.

Like [24,27], the proposed work considers the impact of process and environmental variations on waveforms. In the proposed work, the basis functions are derived by PCA. Hence, the proposed approach extends prior work in [25,26] by including in PCA waveform model construction for large variations from parameters related to the process and the environment. This work formalizes, generalizes, and specifies restrictions for the approach, and proposes methods to make the waveform models practical.

The cell models differ from prior work on modeling cells as equations [10,11,28–30] since the cell models operate on parameters that describe waveforms, not just process parameters, waveform slew, and environmental parameters. The parameters are not required to be independent, and the compact model consists of multivariate polynomials with a minimum number of terms, which are selected based on analysis of variance and accuracy.

Since cells operate on waveforms in the PCA domain, several new problems arise. First, we need to determine the set of PCSs that correspond to realistic waveforms, i.e. PCSs that can be transformed back to the time domain. Second, we need common principal component basis functions for both the inputs and outputs of cells. This is because PCA is a data-driven methodology. Hence each set of input waveforms and each standard cell can generate a unique set of principal component basis functions describing the output waveforms. Hence, some additional steps are needed to come up with a common set of basis functions for all inputs and cells.

Additionally, for our model involving PCA waveform modeling and cell characterization with equations, we show that unlike the tabular static timing analysis method, where memory usage increases exponentially as a function of accuracy in the discretization of parameters that characterize the input and output waveforms (slope and fanout), our proposed method is typically quadratic in memory usage as a function of the parameters describing the waveforms, process, and environmental variations. Finally, we apply the PCA model to static timing analysis and examine the accuracy of delay calculations for long chains of gates.

This paper is organized as follows. Section 2 describes the experimental platform and the parameters modeling variability for cells and waveforms. Sections 3 and 4 discuss waveform model construction and accuracy analysis, respectively. Section 5 describes cell model construction and evaluates accuracy of delays of paths in comparison with Hspice [31] and tabular static timing analysis. Memory usage and computational complexity are summarized in Section 6, followed by a conclusion in Section 7.

2. The experimental platform and model of variation

Traditionally, input waveforms are represented by delay–slope pairs. In this work, the slope is replaced by a set of PCSs. The number of PCSs determines the accuracy of the model. In one extreme, if all the scores are used, the model can reconstruct the exact waveform.

An inverter, designed and layed out with TSMC 180 nm technology, was used to develop the methodology. This technology was the most advanced one available for our CAD tools. After DRC[1] and LVS,[2] parasitics were included in the model through parasitic extraction [32]. Advanced features of Hspice automated the large number of simulation runs, which included generating input waveforms based on a model and capturing the data points of the output waveforms at predetermined relative voltage intervals. The dataset was imported and manipulated using Matlab [33] to construct the two-level full factorial model [34] for each output parameter. The significant effects were determined to form the compact models.

Timing characteristics of standard cells are primarily a function of loading capacitance (fanout), the input waveform, variations of device parameters, i.e., the channel lengths and the threshold voltages of transistors, and the environment, i.e., the power supply voltage and temperature. The ranges of parameters in the model are listed in Table 1. These parameters include the fanout, parameters that describe the input waveform (either slope or principal components, [PC1,PC2] or [L,Θ], described in Section 3), the gate length and threshold voltage of the NMOS and PMOS transistors, temperature, and supply voltage.

The ranges for process parameters were chosen to be small relative to realistic die-to-die process parameter variations, which are on the order of $\pm$30%. This is because die-to-die variation is effectively handled with corner models, and the focus of this work is to supplement these models with variation-aware compact models at each corner that can account for within-die variation, whose range is smaller than die-to-die variation.

[1] Design rule check.
[2] Layout versus schematic.