INTEGRATION, the VLSI journal 42 (2009) 340–345

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

An MTCMOS technology for low-power physical design ☆

Qiang Zhou, Xin Zhao, Yici Cai *, Xianlong Hong

Department of Computer Science and Technology, Tsinghua University, Beijing 100084, PR China

ARTICLE INFO

Article history:
Received 7 January 2008
Received in revised form
5 September 2008
Accepted 5 September 2008

Keywords:
MTCMOS
Low power
Placement
Physical design

ABSTRACT

Multi-threshold CMOS (MTCMOS) technology is an effective sub-threshold leakage power reduction method in CMOS circuits, which satisfies high-performance and low-power design requirements. The optimization of virtual supply network plays an important role in MTCMOS low-power design. Existing low-power works are mainly on gate level, without any optimization on physical design level, which can lead to a large amount of virtual supply networks. Merging the objective of virtual networks minimization into physical design, this paper presents (1) a low-power-driven physical design flow; (2) a novel low-power placement to simultaneously place standard cells and sleep transistors; and (3) the sleep transistor relocation technique to further reduce the virtual supply networks. Experimental results are promising for both achieving up to 28.15% savings for virtual supply networks and well controlling the increase of signal nets.

© 2008 Elsevier B.V. All rights reserved.

1. Introduction

Leakage power is considered to be a great challenge in low-power designs [1–3]. Multi-threshold CMOS (MTCMOS) have been proposed to reduce the leakage by inserting high-threshold sleep transistors to low-threshold circuitry [4]. Fig. 1 shows the schematic of an MTCMOS circuit with N-type sleep transistors. The ground rails of logical gates are connected to the virtual ground networks, which have a potential slightly higher than real ground. The real and virtual ground networks are then linked by the sleep transistors. In the active mode, sleep transistors are turned on, and the virtual ground lines almost function as real ground. In the standby mode, sleep transistors are turned off, and the leakage current is low.

In the previous works on MTCMOS, several strategies have been proposed on gate-level power consumption design [5–9]. Gate clustering in [5] is proposed to cluster different low V_{th} logical gates into sleep transistors in order that simultaneous currents flowing from logical gates to sleep transistors satisfy the tolerance of maximum currents of the given size of sleep transistor. In these clusters, each sleep transistor shares a common virtual network with the logical gates in the same cluster. Modeling sleep transistors as a linear resistor, different sleep transistors sizing methods [6–8] are proposed for performance, noise, and power management. In gate level, the physical location of each gate has not been decided yet. And the minimization of virtual ground network, an equally important design criterion, has been overlooked. Thus, low-power gate-level design with the MTCMOS technique cannot be realized to reduce the virtual supply network.

The existing methods focus at sizing and clustering the sleep transistors [5–9], without a close consideration of the virtual supply networks reduction, which can result in serious interconnect resistance and parasitic capacitance effects on circuit performance [9–11]. The large RC time constant on virtual supply networks will impact the performance in two ways. For one thing, in the active mode, virtual ground networks provide the current discharging pass for each cells, it will take longer for the virtual ground node to discharge back to ground after a transition. For another thing, as virtual ground is slow to discharge, later gates might be slowed down excessively and operate faster than had there been a smaller parasitic effect on the virtual ground node [9,10]. All of these parasitic effects of virtual networks will impact the circuit performance. Meanwhile, if not considering the virtual supply networks, two gates located far apart will be clustered together, which will augment the routing complexity of the circuit. Therefore, virtual supply network minimization is important to ensure circuit performance in an MTCMOS design.

Impacts of virtual ground parasitic are analyzed in [11] works. Also Anis et al. [10] and Babighian et al. [12] have proposed post-layout gate clustering, and sizing methods, and put the physical location of gates into cost function. But there are still three disadvantages for the indirect minimization of virtual ground network after traditional placement. Firstly, traditional placement

☆ This work is supported by National Natural Science Foundation of China (NSFC) 60776026. This paper was presented in part at the Proceedings of International Symposium on Circuits and Systems 2006 [14].

* Corresponding author.
E-mail address: caiyc@mail.tsinghua.edu.cn (Y. Cai).

0167-9260/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.vlsi.2008.09.004

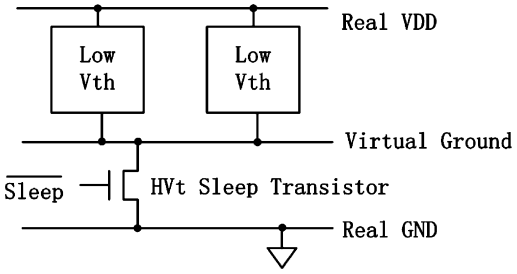

Fig. 1. Schematic of MTCMOS.

takes only interconnect wire length into consideration without virtual ground network objective and thus the virtual ground networks have not yet been minimized in placement. There will be a large amount of virtual ground length after traditional placement. Secondly, the location of each gate is confirmed after placement. The lengths of virtual grounds would maintain the large parasitic RC time constants despite the methods in post-layout. Lastly, sleep transistors are not placed together with other logical gates, but in the additional cavities specially designed for them. This layout largely increases the total chip area and net congestion, and is not flexible for gate clustering and virtual ground networks construction.

Low-power design in the post-layout level mainly includes the fixed-row-based sleep transistors' placement [10,12]. These low-power post-layout design methods first obtain the physical location of gates from existing physical design tools without considering the virtual supply networks minimization, and then put this physical information into cost function to place sleep transistors. In the fixed-row-based methods, sleep transistors are not placed together with other logical gates [7,10], but in the additional cavities specially designed for them. This method largely increases the total chip area and net congestion. And it is not flexible for circuit performance optimization.

In this paper, we propose a novel low-power-driven physical design method and placement techniques to deal with low-power implementation. They can not only reduce the virtual supply network to optimize the circuit performance but also address the problems of sleep transistor sizing and clustering, thus taking full advantage of the MTCMOS low-power technique.

The contributions of this paper are outlined as follows:

- A novel physical design method with low-power requirement is proposed to provide the flexible layout for simultaneously placing standard cells and sleep transistors, which can obtain a minimum area and improve the circuit performance.
- The low-power placement technique as *net weighting balance* is provided to trade off two objectives of signal nets and virtual supply networks minimization by assigning different weights to the signal nets and virtual supply networks.
- The low-power placement technique as *sleep transistor relocation* is proposed to further reduce the virtual supply networks by placing sleep transistors in optimal locations.

From another point of view, we know that two of the most important aspects that contribute to ground bounce are the resistance and capacitance on virtual ground network. Large resistance and capacitance usually lead to serious ground bounce effect. The reduced virtual ground wire length can result in smaller interconnect resistance and parasitic capacitance. So we believe our approach can also relieve the ground bounce effect by significantly reducing virtual ground wire length.

The rest of the paper is organized as follows. Problem formulations are described in Section 2. The low-power physical design flow is outlined in Section 3. In Section 4, the low-power placement with two techniques as net weighting balance and sleep transistor relocation are described. We present the experimental results of this new methodology in Section 5, and conclude the paper in Section 6. To our knowledge, it is the first low-power design method in physical design level to achieve virtual networks minimization in the MTCMOS technique.

2. Problem formulation

2.1. Preliminary

A *Sleep Transistor Cluster* (*ST cluster* for short) is composed of a sleep transistor and the corresponding logic gates that can be turned off in the sleep mode. Referring that N-type sleep transistor provides a virtual ground to the gates connecting to it, we denote this virtual supply line as *virtual ground network* (*Vnet* for short). To distinguish sleep transistor (*ST* for short), *Normal cell* (*Ncell* for short) is the general term for the logical gate. And, *signal net* (*Snet* for short) is used to denote the logic connection between normal cells.

Fig. 2 gives an example. Gates 1–4 are denoted as $Ncell_1$ to $Ncell_4$, which are connected by signal nets, named $Snet_A$ to $Snet_D$ as illustrated in Fig. 2A. Considering the switching currents, $Ncell_1$ and $Ncell_3$ are proposed to be clustered with sleep transistor ST_1, and $Ncell_2$ and $Ncell_4$ are clustered with ST_2. As shown in Fig. 2B, the virtual ground network for ST_1 is constructed by virtual nets $Vnet_{VA}$ and $Vnet_{VB}$, which supply virtual ground for $Ncell_1$ and $Ncell_3$. And $Vnet_{VC}$ and $Vnet_{VD}$ are the virtual ground networks for $Ncell_2$ and $Ncell_4$. $Ncell_1$ and $Ncell_3$ as well as ST_1 form one *ST cluster*, and $Ncell_2$ and $Ncell_4$ together with ST_2 form another one.

2.2. Low-power placement

In post-layout low-power design [10], extra cavities between each pair of standard cell row and power supply row are used, which are specially designed for *ST*s. This fixed-row-based method brings large area as well as congestion problem. In our proposed low-power physical design method, the *ST*s, along with *Ncells*, are placed in the standard cell rows. It not only saves routing area but also is more flexible for *Vnets* optimization.

2.2.1. Formulation

Low-power placement (*LPP*): Given the normal cells and sleep transistors with their signal netlists and virtual ground networks, *LPP* is to find a placement by simultaneously adjusting the physical location of normal cells and sleep transistors so that both the signal nets' length and the virtual ground network length are minimal.

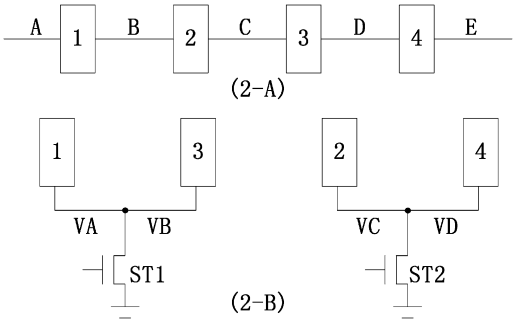

Fig. 2. Circuit example.

Download English Version:

https://daneshyari.com/en/article/540194

Download Persian Version:

https://daneshyari.com/article/540194

Daneshyari.com