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PIXAR: A performance-driven X-architecture router based on a novel multilevel framework

Tsung-Yi Ho *

Department of Computer Science and Information Engineering, National Cheng Kung University, Tainan, Taiwan

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ABSTRACT

As technology advances into the nanometer territory, the interconnect delay has become a first-order effect on chip performance. To handle this effect, the X-architecture has been proposed for high-performance integrated circuits. In this paper, we present a performance-driven X-architecture router based on a novel multilevel framework, called *PIXAR*. To fully consider performance-driven routing and take advantage of the X-architecture, PIXAR applies a novel multilevel routing framework, which adopts a two-stage technique of top-down uncoarsening followed by bottom-up coarsening, with a trapezoid-shaped track routing embedded between the two stages to assign long, straight diagonal segments for wirelength reduction. We also propose a performance-driven X-Steiner tree algorithm based on the delaunay triangulations to construct routing tree for performance optimization. Compared with the state-of-the-art work, PIXAR achieves 100% routing completion for all circuits while reduced the net delay.

1. Introduction

As integrated circuit geometries shrink to 90 nm and below, interconnect delay has become the dominant factor in determining circuit performance. To minimize interconnect delay, two key IC technologies have been introduced: (1) copper and low-k dielectrics have replaced aluminum (as of the 180-nm and 130-nm nodes), reducing both resistance and capacitance, and (2) the ICs have been adapted to a new interconnect architecture, called the *X-architecture*, to shorten interconnect length and, thus, circuit delay.

The traditional Manhattan architecture has its obvious advantages of easier design (placement, routing, etc), but it adds significant and needless wirelength over the Euclidean optimum. As reported in [19], the average Manhattan wirelength is significantly longer than the average Euclidean distance. As shown in [15,18,20], the X-architecture's pervasive uses of diagonal routing can reduce wirelength and via count. In addition, the wirelength and via count reduction make the routing problem easier to solve, resulting in faster timing closure. These benefits contribute towards an increased probability of first-silicon success.

The continuously increasing design complexity imposes severe challenges for modern routers. To cope with the increasing complexity, researchers have proposed multilevel approaches to handle the problem [5,7,8,11–13,16]. All of the previous multilevel frameworks adopt a two-stage technique, bottom-up coarsening followed by top-down uncoarsening. These frameworks handle the target problems first bottom-up from local configurations to global ones and then refine the solutions top-down from global to local. It is obvious that there are significant limitations for this framework to handle the global circuit effect, such as interconnection optimization, since only local information is available at the beginning stages. A wrong choice made in such early stages may make the solution very hard to be refined during the top-down stage.

Ho et al. proposed a pioneering multilevel routing approach for the X-based architecture [13]. Their multilevel routing framework adopts the traditional multilevel routing framework of coarsening followed by uncoarsening, with a trapezoid-shaped track assignment embedded between these two stages. Recently, Chang and Chang [5] present a novel multilevel framework for full-chip routing using the X-architecture, called *X-Route*. Unlike the traditional multilevel frameworks that apply bottom-up coarsening followed by top-down uncoarsening, their multilevel framework adopts the two-stage technique of top-down uncoarsening followed by bottom-up coarsening.

In this paper, we present a performance-driven X-architecture router based on a novel multilevel framework, called *PIXAR*. PIXAR presents several novel techniques that make the recently published multilevel routing scheme for the X-based architecture [13] more effective and complete. Different from the

* Tel.: +886 6 275 7575; fax: +886 6 274 7076.
E-mail address: tyho@csie.ncku.edu.tw

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aforementioned works, PIXAR has the following distinguished features:

- A performance-driven multilevel routing framework, which adopts a two-stage technique of top-down uncoarsening followed by bottom-up coarsening, with a trapezoid-shaped track assignment embedded between the two stages to assign long, straight diagonal segments for wirelength reduction.
- A performance-driven X-Steiner tree (PDXST) algorithm based on the delaunay triangulations to construct routing tree for performance optimization.
- A double fan-out X-detailed router is applied for not only better routing completion but also runtime and memory reduction.

Different from the previous multilevel X-routing framework, PIXAR adopts a four-stage technique of a trial routing stage, followed by a top-down uncoarsening stage with congestion-driven global pattern routing, with an intermediate track routing stage, and then followed by a bottom-up coarsening stage with double fan-out X-detailed routing. Fig. 1 shows the new multilevel X-routing framework of PIXAR.

To fully consider performance-driven routing and take advantage of the X-architecture, PIXAR first runs the PDXST algorithm to construct routing tree for decomposing each net into 2-pin connections, with each connection corresponding to an edge of the PDXST. PIXAR then pre-estimates the congestion in the multilevel X-routing graph for all 2-pin connections by building the congestion map. By the guidance of the trial routing stage, our new multilevel framework starts from uncoarsening the coarsest tiles of the highest level. At each level, we performs congestion-driven global pattern routing for global nets and then refine the solution for the next level. After the uncoarsening stage, we perform trapezoid-shaped track routing to assign long, straight diagonal segments for wirelength reduction. After that, the coarsening stage starts by performing double fan-out X-detailed router to reroute failed nets and refine the solution level by level for better routing completion rate. This new framework outperforms the traditional one [13] in optimizing global circuit effects, since it first considers the global configuration and then processes down to local ones level by level and, thus, the global effects can be handled at earlier stages. Compared with the state-of-the-art work, PIXAR achieves 100% routing completion for all circuits while reduced the net delay.

The rest of this paper is organized as follows. Section 2 presents the routing model for the multilevel routing framework. Section 3 presents our novel multilevel routing framework for the X-architecture. Experimental results are shown in Section 4. In Section 5, we conclude our work and suggest future directions for research.

2. Preliminaries

2.1. Multilevel X-routing model

We model the routing resource as a routing graph whose topology can represent the chip structure. Fig. 2 illustrates the graph modeling. For the modeling, we first partition a chip into an array of octagonal subregions, each of which may accommodate tens of routing tracks in each dimension. These subregions are usually called *global cells* (*GCs*). An octagon in the graph represents a *GC* in the chip, and an edge denotes the boundary between two adjacent *GCs*. Edge length of octagons are used to represent the capacity between *GCs*. Then we add some diagonal edges to connect each two diagonally adjacent octagons to obtain the

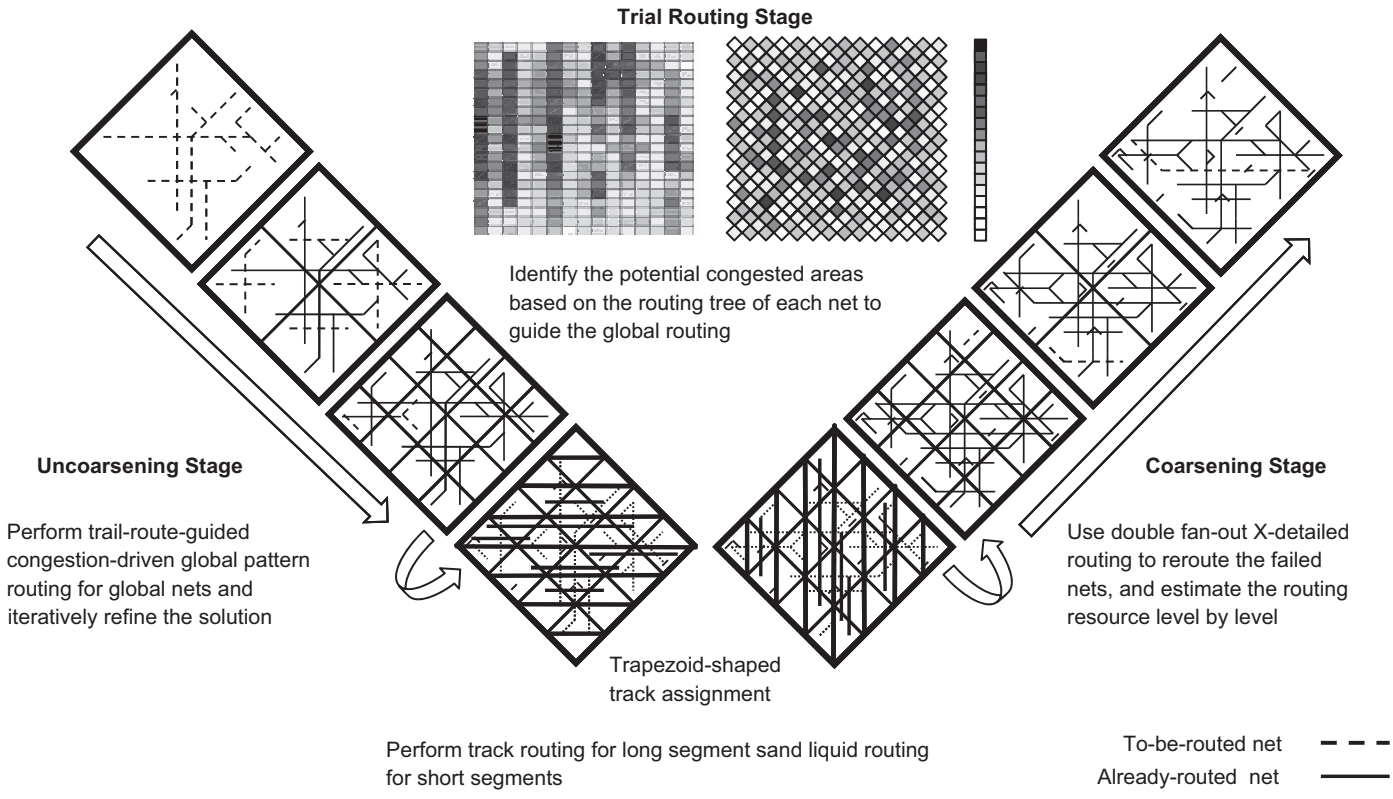

Fig. 1. The multilevel X-routing framework of PIXAR.