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Hetero- and homo-epitaxial growth of 3C-SiC for MOS-FETs

H. Nagasawa *, K. Yagi, T. Kawahara, N. Hatta, M. Abe

HOYA Advanced Semiconductor Technologies Co. Ltd., 1-17-16 Tanashioda, Sagamihara, Kanagawa 229-1125, Japan

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Abstract

Planar defects, like anti-phase boundaries (APBs) and stacking faults (SFs), are reduced by growing 3C-SiC on undulant-Si whose entire surface is covered with countered slopes oriented in the [1 1 0] and [$\bar{1}\,\bar{1}$ 0] directions. During the initial 3C-SiC growth, APBs are eliminated on each slope of an undulation. Then, one kind of SF self-vanishes. However, another kind of SF remains on the 3C-SiC surface, although its density is gradually reduced with increasing SiC thickness by combining with a counter-SF. The leakage current of a pn diode fabricated homo-epitaxially on 3C-SiC is roughly proportional to the SF density before homo-epitaxial growth. The viability of 3C-SiC grown on undulant-Si for semiconductor devices is discussed by reviewing recent reports on various MOS-FETs using it as the substrate. The key issue in the fabrication of a MOS-FET as a power-switching device operated at high-voltage is to reduce the leakage-current at the pn junction, thereby eliminating SFs.

Keywords: 3C-SiC; Anti-phase boundary; Stacking fault; MOS-FET; pn junction, Homo-epitaxy; Hetero-epitaxy

1. Introduction

3C-SiC has advanced electrical properties, like high low-field electron mobility and high saturated electron drift velocity [1,2]. Concerning its application as a power switching device, we have to emphasize that the small donor ionization energy in 3C-SiC and low interface state density at SiO_2/3C-SiC are a crucial advantage for obtaining high-performance metal-oxide-semiconductor field-effect transistors (MOS-FETs) [3,4]. Despite these advantages, applications using 3C-SiC have lagged significantly behind those using hexagonal-type SiC, due to the large leakage current at the pn junction via planar defects or dislocations [5]. In order to reduce the density of planar defects, we developed a technology for growing 3C-SiC on an undulant-Si substrate [6–8].

This paper first introduces a mechanism for reducing planar defects when 3C-SiC is grown on undulant-Si. Next, the leakage-current at pn junctions formed homo-epitaxially on 3C-SiC substrate with various SF densities is reported, in order to clarify the effect of SFs on the device characteristics. Finally, the feasibility of 3C-SiC as a substrate for power semiconductor devices is discussed by referring to recent reports that describe MOS-FET fabrication using 3C-SiC grown on undulant-Si substrate.

2. Reduction of planar defects in 3C-SiC through hetero-epitaxial growth on undulant-Si

The planar defects in 3C-SiC grown on Si(0 0 1) substrate can be classified into two main types: anti-phase boundaries (APBs) and stacking faults (SFs). An APB in 3C-SiC is the interface between two domains that correspond to each other through the exchange of Si and C atoms and it inevitably consists of Si–Si or C–C bonds along the {1 1 1} planes. Conversely, a SF in 3C-SiC can be regarded as hexagonal sites inserted along the {1 1 1} planes, to minimize the number of dangling bonds at the SiC/Si interface.

We investigated a technique that involves growing 3C-SiC on undulant-Si to reduce the SFs and APBs simultaneously. Fig. 1 is an atomic force microscope (AFM) image of the surface of typical undulant-Si. The AFM image exhibits continuous undulations with ridges roughly

* Corresponding author. Tel.: +81 42 777 5405; fax: +81 42 777 5406/425 46 2742.
E-mail addresses: nags@hast.co.jp, nags@rdc.hoya.co.jp (H. Nagasawa).

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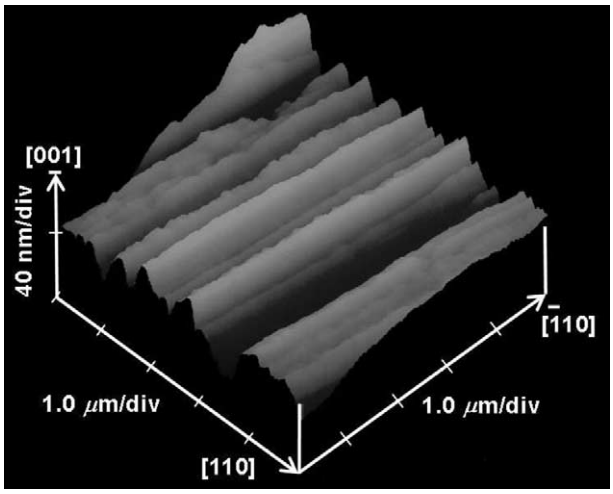

Fig. 1. AFM image of surface of typical undulant-Si: The interval between adjacent ridges is 400–700 nm, and the height-difference between ridges and valleys is 7–26 nm.

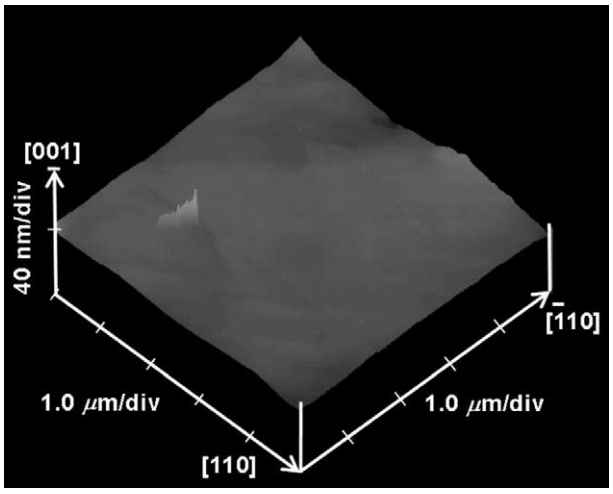

Fig. 2. AFM image of surface of 3C-SiC grown on undulant-Si: The surface is much smoother than that of the undulant-Si surface, suggesting that the growth rate of 3C-SiC is higher in lateral than in vertical.

paralleling the [$\bar{1}$10]-direction formed on the Si(001) substrate. The interval between adjacent ridges is 400–700 nm, and the height-difference between ridges and valleys is 7–26 nm [7].

A 3C-SiC hetero-epitaxial layer is grown on the undulant-Si using a cold-wall-type, low-pressure CVD system. Before SiC growth, the surface of the undulant-Si is carbonized in a C_2H_2 environment at an elevated temperature for 5 min, in order to maintain the fine structure of the undulant-Si surface. Then, the 3C-SiC hetero-epitaxial layer is grown on a carbonized layer using SiH_2Cl_2, C_2H_2, and H_2. During the carbonization and growth processes, the temperature of the substrate is controlled at 1623 K, which is just below the melting point of Si. Using this procedure, hetero-epitaxial 3C-SiC about 200-μm thick is grown on the undulant-Si for 5 h. Details of the process of preparing for undulant-Si and SiC growth conditions are described elsewhere [6,7].

The surface of the 3C-SiC grown on the undulant-Si is much smoother than that of the undulant-Si surface, as shown in the AFM image in Fig. 2. This suggests that the growth rate of 3C-SiC is higher in the [110] or [$\bar{1}\bar{1}$0] directions (lateral growth) than in the [001] direction (vertical growth), and therefore, it is obvious that APB can be eliminated via step-flow on the slopes of the undulant-Si surface. This mechanism is quite similar to that reported on misoriented-Si [9]. In addition, SFs can be also reduced as described below. A SF region is a triangular plate, as shown schematically in Fig. 3, and it aligns coherent boundaries in the {111} planes. By contrast, incoherent boundaries of SFs, which correspond to dislocations, propagate linearly in the {110} planes, to maintain their polarity to be Si-face. As a result, SFs that expose their C-face at the (001) surface (Fig. 3(a)) rapidly disappear with increasing 3C-SiC thickness, while SFs that expose their Si-face (Fig. 3(b)) expand. Consequently, only SFs that expose their Si-face on the (001) surface remain in the 3C-SiC surface. However, in the APB-free 3C-SiC surface, they are arranged symmetrically in the ($\bar{1}$11) or (1$\bar{1}$1) planes, as shown in Fig. 3(b), and reduce their density gradually by combining with counter-SFs with increasing 3C-SiC thickness [7,8]. Therefore, the SF density at the 3C-SiC surface grown on undulant-Si is roughly inversely proportional to the thickness. In other words, the thicker the 3C-SiC surface, the lower the SF density.

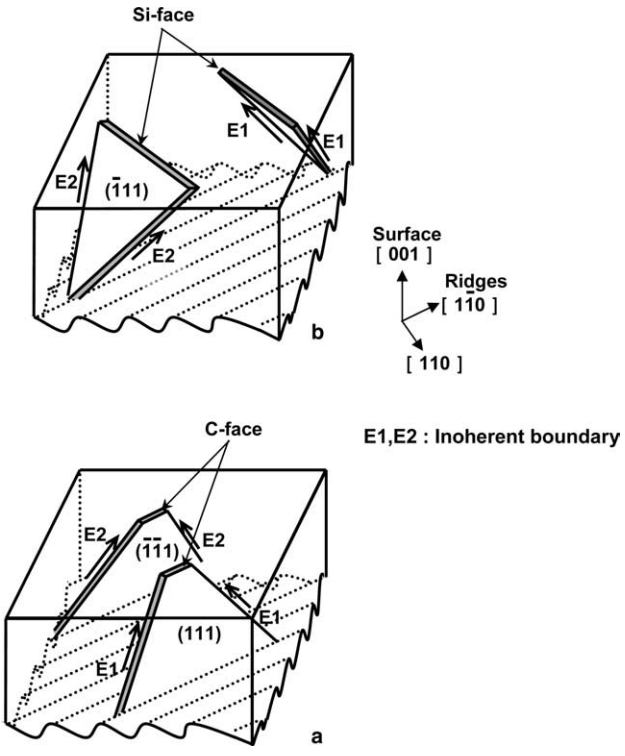

Fig. 3. Schematic view of stacking faults (SFs) in 3C-SiC grown on undulant-Si: (a) SFs that expose C-face at the surface and (b) SFs that expose Si-face.