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A new approach to power estimation and reduction in CMOS digital circuits

Ireneusz Brzozowski*, Andrzej Kos

AGH University of Science and Technology, Institute of Electronics, Al. Mickiewicza 30, 30-059 Cracow, Poland

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Abstract

Modelling and optimization of dynamic capacitive power consumption in digital static CMOS circuits, taking into consideration a reason of a gate switching—*gate control mode*, is discussed in the present paper. The term 'gate control mode' means that a number and type of signals applied to input terminals of the gate have an influence on total amount of energy dissipated during a single switching cycle. Moreover, changes of input signals, which keep the gate output in a steady state, can also cause power consumption. Based on this observation, complex reasons of power losses have been considered. In consequence, the authors propose a new model of dynamic power consumption in static CMOS gates. Appropriate parameters' calculation method for the new model was developed. The gate power model has been extended to logic networks, and consequently a new measure of the circuit activity was proposed. Switching activity, which is commonly used as a traditional measure, characterizes only the number of signal changes at the circuit node, and it is not sufficient for the proposed model. As the power consumption parameters of CMOS are dependent on their control mode, the authors used *probability of the node control mode* as a new measure of the circuit activity. Based on the proposed model, a procedure of combinational circuit optimization for power dissipation reduction has been developed. The procedure can be included in a design flow, after technology mapping. Results of the power estimation received for some benchmark circuits are much closer to SPICE simulations than values obtained for other methods. So the model proposed in this study improves the estimation accuracy. Additionally, we can save several percent of the consumed energy.

Keywords: Power consumption modelling and estimation; Static CMOS logic; Circuit optimization; Parameter estimation; Inputs reordering; Gate control mode

1. Introduction

Power dissipation in VLSI circuits is one of the most important performance parameters occurring during today's design process. Due to continuous scaling down, the power consumed by a chip is one of the largest power densities occurring in the world [1]. It has a strong influence on the VLSI design efficiency and reliability. It also limits speed and lifetime of portable devices, etc. Temperature gradients occurring in an integrated circuit are sources of harmful thermomechanical stresses and can consequently result in the chip damage. Therefore, understanding of power dissipation reasons and appropriate estimation of consumed energy in VLSI chips is very important. In the case of CMOS digital circuits, which are commonly present in today's VLSI systems, all consumed power is dissipated as heat. So, the new models describing behaviour and properties of CMOS circuits, especially in the light of fast development of submicron technology, are needed. Universal models of electronics components, which are independent of the technological process, as well as design methods, are willingly used by designers. These make their work more comfortable, while designs are more universal, and easier transferred to new technologies.

Many authors of the papers in question use the commonly known capacitive model of dynamic power dissipation in CMOS circuits [2,3]. In this model, the effective node capacitance and switching activity are

*Corresponding author. Tel./fax: +48 12 6332398.
E-mail addresses: brzoza@agh.edu.pl (I. Brzozowski), kos@agh.edu.pl (A. Kos).

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usually used. The capacitance consists of the gate fan-out and fan-in of next gates as well as of the interconnection capacitance. The capacitance can be evaluated based on a layout extraction and transistor parameters or on simulations [4–6]. But the capacitance value is still constant and is independent of the control mode of a gate. On the other hand, studies on short-circuit power dissipation modelling have been developed [7,8]. In the pioneer studies [2,9], the short-circuit power dissipation was neglected. It is the proper assumption for well-designed circuits [10]. Considering capacitance of internal nodes of a gate and switching activity of input signals, some works concerning reduction of power dissipation by reordering of transistors/inputs have been developed [11,12].

Detailed analysis of CMOS gates behaviour during switching, as well as measurements of the consumed power in real circuits, executed by authors, shows that the dynamic power dissipation of the CMOS gate depends on switching reason. Moreover, energy is consumed even when the gate output does not change its logical state while the input signals are changed. It happens when the gate is controlled without switching. Hereby, the authors' intention is to propose a versatile model of dynamic capacitive power dissipation of CMOS gates and logic circuits taking into account the dependencies mentioned. Based on the proposed model, power dissipation of a circuit can be accurately estimated and improved.

The idea was partly presented on MIXDES conferences [13,14]. Reasons and dependencies of power dissipation in static CMOS circuits are discussed in brief Section 2 of the paper. Analyses and measurements presented in Section 3 tempted the authors to write the present study. In the next section, a description of the proposed power model of gate is introduced. Theoretical background of gates energy properties assessment is discussed in Section 5. In this section, methods and results of dynamic energy properties assessment for a few basic CMOS gates are also presented. An example of power consumed by a simply logic network is presented in Section 6, where results of power estimation for a set of benchmark circuits are also discussed. Section 7 describes the optimization method for combinational circuits in the aspect of power reduction while the proposed model is used. Optimization results of a set of MCNC benchmark circuits, using proposed procedure, are also presented. Section 8 summarizes the studies and suitable conclusions are drawn.

2. Power dissipation in static CMOS circuits

2.1. Sources of power dissipation

Power dissipation in a static CMOS circuit is directly related with its actual state. So, we can distinguish its static component when the gate remains idle and dynamic one when it is put in operation. The static losses are generated due to leakage currents: reverse-biased p–n junctions, transistor gate, subthreshold, etc. And the losses become even more significant in submicron technologies [15]. During input voltage transition of the gate, the current flows from a supply rail to the ground through the gate, according to the quasi-short path. The second component of dynamic energy losses is related to current paths resulting from charging or discharging of the internal gate capacitors and an external load. In the present study, our attention was focused on dynamic capacitive power consumption considered as the main part of energy losses in CMOS circuits.

2.2. Power dissipation dependencies

The dynamic and quasi-short components of CMOS circuits power dissipation depend on a few parameters, which can be divided into two groups. The internal parameters depend on the technology and layout design of a gate. For example, sizes of MOS transistors have influence on the value of quasi-short current as well as on internal capacitances (junction capacitance of diffusion layers, oxide capacitance, etc.). Therefore, for a given set of gates, their internal energy parameters can be assessed. On the other hand, power consumed by the gate also depends on external parameters such as the shape and duration of input voltage, activity of input signals, or more precisely, on the gate control mode (type and number of signals applied at the gate inputs), and of course, on the external load capacitance (i.e. interconnections and inputs of next gates). Based on these dependencies, a designer of digital circuits or systems, using a given library of gates, can influence the power dissipation in the circuit by choosing an appropriate method of gates connection.

3. Motivation

Capacitive model of power dissipation in CMOS digital circuits, which is usually used, is based on constant values of capacitors used. But, in fact, capacitance representing power dissipation depends on a gate control mode. In order to prove this statement, authors made the following measurements, based on a testing circuit shown in Fig. 1.

During the tests, supply current of the first gate (NOT) was measured. One of the inputs of the second gate (NAND) was driven by the NOT, but for the remaining ones logic 0 and/or 1 were applied. Four following cases were taken into account (00, 01, 10, 11). So, input capacitance of the input A was measured versus different control modes of the NAND gate. Authors used two fabricated chips with several types of static CMOS gates [16]. The chip was designed by Microelectronics Systems Design Group at the AGH-UST Institute of Electronics. The chip was designed for the power dissipation investigations in static CMOS gates, using AMIS CMOS 0.7 μm C07M-D technology [17]. The integrated module consists of four gate types: NOT, 2- and 3-input NAND, and 3-input NOR. Circuits in the chip were designed as blocs of 100 gates connected in parallel, in order to increase the