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Ge metal-oxide-semiconductor devices with $Al_2O_3/Ga_2O_3(Gd_2O_3)$ as gate dielectric

L.K. Chu [a], T.H. Chiang [a], T.D. Lin [a,d], Y.J. Lee [a], R.L. Chu [a], J. Kwo [b,c,*], M. Hong [d,*]

[a] Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan
[b] Department of Physics, National Tsing Hua University, Hsinchu 30013, Taiwan
[c] Center for Condensed Matter Science, National Taiwan University, Taipei 10617, Taiwan
[d] Department of Physics and Graduate Institute of Applied Physics, National Taiwan University, Taipei 10617, Taiwan

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ABSTRACT

$Ga_2O_3(Gd_2O_3)$ [GGO] 3.5 nm-thick, with an *in situ* Al_2O_3 cap 1.5 nm thick, has been directly deposited on Ge substrate without employing interfacial passivation layers. The equivalent oxide thickness (EOT) of the gate stack is 1.38-nm. The metal-oxide-semiconductor (MOS) capacitors using Al_2O_3/GGO as the gate dielectric have given capacitance–voltage characteristics with frequency dispersions of ~4% at accumulation (10 kHz–1 MHz) and frequency dependent flat-band voltage shift (~30 mV). The dielectric constant of the GGO remains at 14–15. Furthermore, the TiN/Al_2O_3/GGO/Ge pMOSFET with a gate length of 1 μm has given a saturation drain current density, a maximum transconductance and a field-effect hole mobility of 800 μA/μm, 423 μS/μm, and 300 cm^2/V s, respectively.

When channel materials other than Si are considered to enhance the switching speed of metal-oxide-semiconductor (MOS) transistors, Ge has always been one viable candidate due to its higher carrier mobility than that of Si. Achieving a high-quality interface between high κ dielectrics and Ge is extremely challenging, but is a must to realize high-performance MOS devices. Employing interfacial passivation layers (IPLs) of GeON [1], SiO_2/Si [2], and GeO_2 [3,4] prior to the high κ dielectrics deposition has led to Ge MOS devices with good performance. Particularly, those using GeO_2 have exhibited a low interfacial state of density (D_{it}) and high carrier mobility. However, degradation of GeO_2/Ge interface and diffusion of Ge into the bulk high κ's occurs as GeO_2 becomes thinner, leading to increased defect density; this and relatively low permittivity of GeO_2 (~7) may hinder further scaling of the capacitance equivalent thickness (CET)/equivalent oxide thickness (EOT) [4]. For a technology beyond Si CMOS, a $D_{it} \leqslant$ low 10^{11} cm^{-2} eV^{-1} and a CET/EOT value below 1 nm are adamantly required.

Among approaches without IPLs of depositing high-κ's (HfO_2 [5], Y_2O_3 [6], CeO_2 [7], La_2O_3 [8,9], and $Ga_2O_3(Gd_2O_3)$ [GGO], [10,11]) on Ge(100) in ultra high vacuum (UHV), GGO/Ge has shown good thermal stability withstanding high-temperature anneals at least to 500 °C, exhibiting an atomically abrupt oxide/semiconductor interface with minimized Ge inter-diffusion [12]. Low D_{it}'s of $\leqslant 3 \times 10^{11}$ cm^{-2} eV^{-1} were extracted around the mid-gap after a CF_4/O_2 plasma treatment, consistent with the measured high Fermi-level movement efficiency of 80% [13].

In this letter, we have further reduced GGO thickness to achieve sub-nm CET and studied the GGO/Ge MOS device performance. A GGO 3.5 nm-thick with an *in situ* Al_2O_3 cap (~1.5 nm) for MOS capacitors (MOSCAPs) has given a total EOT of 1.38 nm, attaining a 0.96 nm CET in GGO. A 1 μm (gate length) MOS field-effect-transistor (MOSFET) has exhibited excellent electrical performance of a saturation drain current density of 800 μA/μm, a maximum transconductance of 423 μS/μm, and a field effect hole mobility of 300 cm^2/V s. We showed that the device performances of the Ge pMOSFET based on GGO without IPL as the gate dielectric, compare favorably with those using IPLs.

After dipped in 2% diluted HF solution and rinsed in de-ionized water, 2-in. n-type Ge(100) wafers (Sb-doped) with a resistivity of 0.31–0.34 Ω cm were immediately loaded into a UHV multi-chamber growth/characterization system. By annealing to ~450–500 °C, an atomically ordered Ge surface free of contaminations and residual native oxides was attained, as confirmed by a (2 × 2) reconstructed reflection high energy electron diffraction (RHEED) pattern and characterized by *in situ* X-ray photoelectron spectroscopy (XPS). GGO and the subsequent Al_2O_3 cap were electron-beam evaporated from the oxide targets at room temperature in sequence, with the detailed oxide growth given previously [6,11]. Post deposition treatments (PDTs), using a $CF_4 + O_2$ plasma treatment followed by nitrogen annealing (500 °C for 5 min), has improved the GGO and GGO/Ge interfacial quality [12,13]. Sputter-deposited TiN was utilized as the metal gate. The process flows for fabricating the MOS devices were described elsewhere

* Corresponding authors.
E-mail addresses: raynien@ntu.edu.tw (J. Kwo), mhong@phys.ntu.edu.tw (M. Hong).

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[11,13]. Agilent 4284 and 4156C were used for measuring capacitance–voltage (C–V) and current–voltage (I–V) characteristics, respectively.

After PDTs, the GGO/Ge and its interface remain intact, with the electronic/chemical characteristics investigated using synchrotron radiation photoemission [14], and the microstructures studied by high-resolution transmission electron microscopy (HR-TEM) (Fig. 1(a)). The quality of the gate stack and the GGO/Ge interface was also evaluated using C–V curves (shown in Fig. 1(b)) from the MOSCAPs (inset of Fig. 1(d)). The C–Vs exhibit small frequency dispersion at accumulation and negligible frequency-dependent flat-band voltage shift. In the inversion region, the measured capacitance responds well to the frequencies, i.e. increased capacitance with decreased frequencies. The value of the measured transition frequency (f_t) of ~10 kHz, defined as the frequency where the capacitance is in the middle of maximal and minimal capacitances, is in the same range of the reported value of ~6 kHz [15]. The slightly higher f_t in this work may be attributed to the lower D_{it}'s. The deviation observed from the C–V in the accumulation region at 1 kHz is due to the gate leakage. The C–V hysteresis at 1 MHz was shown in the inset of Fig. 1(c), where the voltage shift between forward and reverse sweeping at flat-band capacitance is ~50 mV. A small frequency dependent flat-band voltage (V_{fb}) shift (10 kHz–1 MHz) of ~30 mV was attained, suggesting low D_{it}'s near the mid-gap energy. A frequency dispersion of ~4% (10 kHz–1 MHz) at accumulation indicates that the interfacial traps are not significant in the upper half of the bandgap [16]. The minor frequency dispersions in both accumulation and depletion regions are in good agreement with the low D_{it}'s of $\sim 10^{11}\ cm^{-2}\ eV^{-1}$ from mid-gap towards conduction band edge, obtained by conductance method carried out from room temperature to 77 K [16].

A capacitance equivalent thickness (CET) of 1.69 nm is extracted from the 1 MHz oxide capacitance (C_{ox}), leading to a κ value of GGO of ~14.3 (using a previously calibrated κ of Al_2O_3 of 8). Taking the quantum mechanical behavior of the carriers into consideration, the EOT of Al_2O_3/GGO was then determined using the NCSU CVC software; the physical oxide thickness, V_{fb}, and substrate doping of the Al_2O_3/GGO/Ge were used to fit the experimental C–V data [17]. Fig. 1(c) shows the experimental and the modeling C–V curves at high and low frequencies, revealing an EOT of 1.38 nm for the bi-layer dielectrics. After subtracting the CET contribution of Al_2O_3, i.e. $\kappa_{SiO_2}/\kappa_{Al_2O_3} \times 1.5\ nm \sim 0.73\ nm$, GGO has a CET of around 0.96 nm. The gate leakage current density (J_g) is also plotted as a function of the electric field (E) as shown in Fig. 1(d). At a gate voltage (V_g) of V_{fb} (0.4 V) + 1 V, J_g is $5.5 \times 10^{-3}\ A/cm^2$, which is about two orders of magnitude higher than that in the sample with only nitrogen annealing at 500 °C for 5 min (not shown). The increase in J_g may be due to the damage caused by the reactive plasma process. Nevertheless, J_g exhibits 3–4 orders of reduction compared to that for SiO_2/Si with the same EOT [18]. Compared to the previous results with thicker GGO layers (>10 nm) [11,13], where a clear soft breakdown field at ± 1–2 MV/cm is observed, the absence of this in Fig. 1(d) indicates that the leakage from the tunneling current, which takes place even at a small electric field due to the thin gate dielectrics.

The drain current density (I_d) vs drain voltage (V_d) of the TiN/Al_2O_3/GGO/Ge pMOSFET with 1-μm gate length (L_g) and 10-μm gate width (W_g) is shown in Fig. 2(a). The measured data are presented as the dotted lines, indicating significant off-state leakages, i.e. linear increase of I_d with increased V_d at V_g = 0. The off-state leakage comes from the source/drain region, which requires further optimization of the implantation/activation process for improvement. After deducting the off-state current, as shown in the solid lines in Fig. 2(a), a saturation I_d of 670 μA/μm at a V_g of −2 V has been attained. As V_g is further increased to −2.5 V, an I_d of ~800 μA/μm has been achieved, along with a maximum transconductance (g_m) of 423 μS/μm at a V_g of −0.9 V, as shown in Fig. 2(b). A maximum hole mobility, extracted from the linear

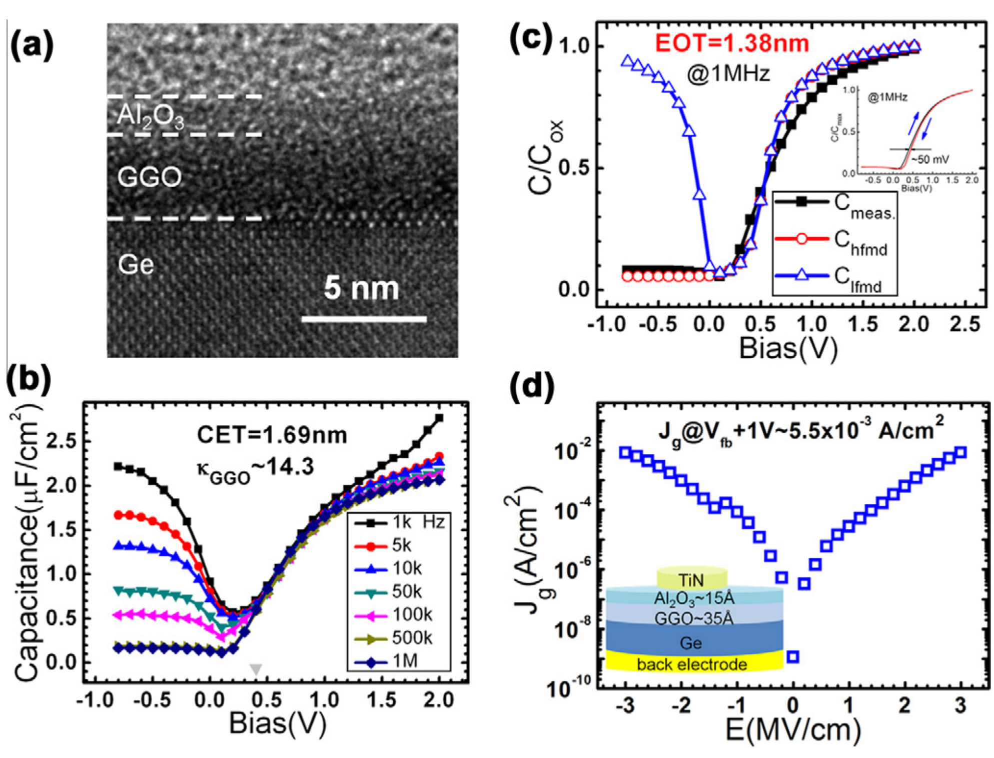

Fig. 1. (a) HR-TEM micrograph of $Al_2O_3/Ga_2O_3(Gd_2O_3)$/Ge(100) after 20 s $CF_4 + O_2$ plasma treatment and 500 °C – 5 min nitrogen annealing. (b) C–V characteristics of the corresponding TiN/Al_2O_3(1.5 nm)/$Ga_2O_3(Gd_2O_3)$(3.5 nm)/n-Ge MOSCAP. (c) Measured C–V data at 1 MHz and the modeling curve at high and low measurement frequencies. The inset shows the C–V hysteresis at 1 MHz. (d) The corresponding J_g–E curve.