Microelectronic Engineering 91 (2012) 154–158

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

On the temperature dependent dielectric properties, conductivity and resistivity of MIS structures at 1 MHz

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ARTICLE INFO

Article history:
Received 18 February 2011
Received in revised form 3 June 2011
Accepted 4 July 2011
Available online 1 October 2011

Keywords:
MIS structure
Dielectric properties
Ac conductivity
Ac resistivity
Electric modulus

ABSTRACT

In this study, the temperature dependence of the dielectric properties, conductivity and resistivity of metal–insulator-semiconductor (MIS) structures have been investigated using capacitance (C) and conductance (G/ω) measurements in wide temperature range of 120–400 K at 1 MHz. Calculation of the dielectric constant (ε'), dielectric loss (ε''), loss tangent ($\tan\delta$), ac conductivity (σ_{ac}), ac resistivity (ρ_{ac}) and the real and imaginary parts of electric modulus (M' and M'') were given in the studied temperature range. The values of the ε', ε'' and σ_{ac} increase exponentially with the increasing temperature between 280 K and 400 K. On the other hand, these values remain almost constant between 120 K and 240 K. In addition, the experimental dielectric data have been analyzed by considering electric modulus formalism. The $\ln\sigma_{ac}$ vs. $1000/T$ plot shows two linear regions with different slopes which correspond to low (120–240 K) and high (280–400 K) temperature ranges. The values of activation energy for two different conduction mechanisms were found as 4 meV and 201 meV for low and high temperature ranges, respectively.

1. Introduction

In metal–insulator–semiconductor (MIS) and metal–oxide–semiconductor (MOS) structures, metal and semiconductor remain separated by an interfacial insulator layer such as SiO_2, Si_3N_4 and TiO_2 and at metal/insulator interfaces there is continuous distribution of surface states with energies located in the band gap of semiconductor. Such an interfacial insulator layer cannot only prevent inter-diffusion between metal and semiconductor, but also alleviate the electric field reduction in MIS structure. Also, semiconductor device parameters such as performance, stability and reliability are highly dependent on the interfacial properties of the interface insulator layer between metal and semiconductor. Because composition and stability of the interface insulator layers is not completely understood, the quality of devices with an interfacial insulator layer is still not satisfactory [1–3].

The existence of such an insulator layer which converts metal–semiconductor (MS) structures into MIS and MOS structures can have a strong influence on the device characteristics as well as the interface states (N_{ss}), and series resistance (R_s) that can modify the electrical properties of MIS structure [4–6].

These interface states usually cause a bias shift in the measured capacitance–voltage (C–V) and conductance–voltage (G/ω–V) curves [7,8]. Series resistance is an important parameter which causes the electrical characteristics of these structures to be non-ideal especially at high bias voltages [9–11]. Therefore, the parameter R_s is only effective in the accumulation region or at sufficiently high bias voltages of the C–V and G/ω–V characteristics at high frequency, whereas the interface states are effective especially in the depletion and weak inversion regions at low frequency. To eliminate the effect of interface states C–V and G/ω–V characteristics were carried out at sufficiently high frequency (1 MHz).

Besides the interfacial insulator layer, the electrical and dielectric properties of MS, MIS and MOS structures are also dependent on some other parameters, such as the process of surface preparation, formation of barrier height at MS interface and its homogeneity, impurity concentration of a semiconductor, density of interface states and dislocations between insulator layer and semiconductor, series resistance of device, applied bias voltage and device temperature. Among them, device temperature is another important parameters which influence both the electrical and dielectric properties of these devices. Therefore, the analysis of electric and dielectric parameters of these devices only at room temperature does not give detailed information about conduction processes. Moreover, the temperature dependence of the C–V and G/ω–V characteristics allows us to understand different aspects of conduction mechanism in these devices.

In our previous studies [12–14], in the first study, we investigated the frequency dispersion in capacitance and conductance in terms of the density of interface states and series resistance in Au/SiO_2/n-Si (MOS) capacitors with 58 Å interfacial insulator layer thickness at room temperature. In the second study, the effect of the frequency and gate bias voltage on dielectric properties of

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0167-9317/$ - see front matter © 2011 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2011.07.016

$Au/SiO_2/n$-Si (MIS) structures with 25 Å interfacial insulator layer thickness was investigated at room temperature. In addition, in the third study, we investigated the analysis of energy density distribution profile of interface states in $Au/SiO_2/n$-Si (MOS) capacitors with 500 Å interfacial insulator layer thickness by using admittance method at room temperature.

Therefore, in this study, we aimed to investigated the temperature effect on dielectric properties of $Au/SiO_2/n$-Si (MIS) structure such as the dielectric constant (ε'), dielectric loss (ε'') and loss tangent ($\tan\delta$) and ac conductivity (σ_{ac}), ac resistivity (ρ_{ac}) and electric modulus in the wide temperature range of 120–400 K at 1 MHz. Experimental results show that knows both the electrical and dielectric properties of MIS structure significantly changes with temperature.

2. Experimental detail

The metal–insulator-semiconductor $Au/SiO_2/n$-Si structures with 79 Å insulator layer (SiO_2) thickness were fabricated on n-type (P-doped) single crystals silicon wafer with ⟨1 0 0⟩ surface orientation, having thickness of 350 μm, 2″ diameter and 1 Ω cm resistivity. For the fabrication process, the Si wafer was degreased in organic solutions of $CHClCCl_2$, CH_3COCH_3 and CH_3OH, then etched in a sequence of H_2SO_4 and H_2O_2, 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF and finally quenched in de-ionized water with resistivity of 18 MΩ cm for a prolonged time. High purity (99.999%) gold (Au) layer with a thickness of ~1500 Å was thermally evaporated from the tungsten filament onto the whole backside of Si wafer at a pressure of $\sim 2\times10^{-6}$ Torr in oil vacuum pump system. The ohmic contact was prepared by sintering the evaporated Au back contact at 650 °C for 60 min in flowing dry nitrogen ambient at rate of 2 l/min. This process served both to the sinter the Au and to form the required insulator layer (SiO_2) on the upper surface of the Si wafer. Finally, circular dots of 1 mm diameter Au with a thickness of ~1500 Å were deposited in order to form the rectifier contacts on the oxidized surface of the Si wafer through a Cu shadow mask in the same vacuum system. The thickness of metal layers and the deposition rates were monitored with the help of quartz crystal thickness monitor. The interfacial layer thickness was estimated to be about 79 Å from high frequency (1 MHz) C–V measurement of the oxide capacitance in the strong accumulation region. In order to carry out C–V and G/ω–V measurements, the electrical contacts are made onto the upper electrode on the oxide with the help of fine phosphor-bronze spring probe.

The capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements were carried out in the temperature range of 120–400 K at 1 MHz, by using a HP 4192A LF impedance analyser (5 Hz–13 MHz) and a small ac test signal 50 mV_{rms} from the external pulse generator was applied to the sample in order to meet the requirement. All measurements were controlled by Janes vpf-475 cryostat, which enables us to make measurements in the temperature range of 77–450 K. The sample temperature was always monitored by using a copper–constantan thermocouple close to the sample and by measuring with a dmm/scanner Keithley model 199 and a Lake Shore model 321 auto-tuning temperature controllers with sensitivity better than ±0.1 K. In addition, all measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

3.1. Temperature dependence of capacitance and conductance at 1 MHz

The conductance technique, which consists of C–V and G/ω–V measurements [7,15], is based on the conductance losses resulting from the exchange of majority carriers at the metal/semiconductor interface and the majority carrier band of the semiconductor when a small ac test signal is applied to the MIS structure.

The variation of the capacitance and conductance with temperature at high frequency (1 MHz) are shown in Fig. 1(a) and (b) for MIS structure, respectively. As shown in Fig. 1(a) and (b), both the C–V and G/ω–V curves increase with the increasing temperature. The capacitance and conductance values are quite sensitive especially at high temperatures. The increase in capacitance and conductance towards high temperature may be due to interfacial space charge formation [16,17].

The existence of interface states at the metal/semiconductor interface acts as recombination centers and create dispersion in capacitance. This interface states can follow the ac signal and yield an excess capacitance, which depends on the temperature and frequency. But, in the high frequency limit ($f \geqslant 500$ kHz), the interface states cannot follow the ac signal. This makes the contribution of interface state capacitance to the total capacitance negligibly small [18]. In this case, the temperature effects become more dominate on the values of C–V and G/ω–V.

3.2. Temperature dependence of dielectric parameters at 1 MHz

The complex permittivity can be defined in the following complex form [19,20]

$$\varepsilon^*(\omega) = \varepsilon'(\omega) - j\varepsilon''(\omega) \tag{1}$$

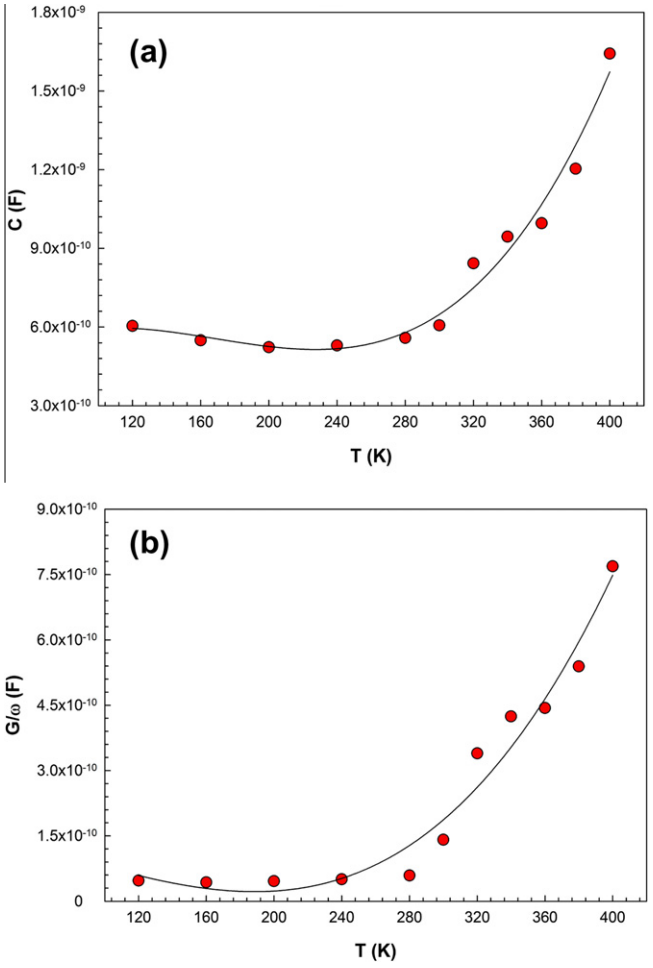

Fig. 1. Variation of the (a) capacitance (C) and (b) conductance (G/ω) with temperature at 1 MHz for MIS structure.