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Moore's crystal ball: Device physics and technology past the 15 nm generation

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ABSTRACT

This paper will discuss advanced CMOS transistor architectures for the 15 nm node and beyond. Transistor architectures such as ultra-thin body (UTB), FinFET (and related architectures such as Trigate, Omega-FET, Pi-FET), and nanowire device architectures will be compared and contrasted. Key technology challenges (such as mobility, resistance and capacitance) shared by all the architectures will be discussed in relation to recent research results. The impact of new transistor architectures on the progression of Moore's Law will be summarized.

1. Introduction

For the past 40 years, relentless focus on Moore's Law transistor scaling has provided ever-increasing transistor performance and density. An excellent example is provided by SRAM scaling over the last five generations, where steady adherence to Moore's Law has delivered 2X bitcell area scaling each generation (see Fig. 1).

As we look forward to the 15 nm node and beyond, there are a number of critical challenges to be addressed. These challenges include reducing the effective gate length (L_{eff}), reducing the gate pitch, and targeting the threshold voltage (V_T).

Reducing L_{eff} is a critical challenge for advanced technology generations. Increased off-state current (I_{off}) from degraded drain-induced barrier lowering (DIBL) and subthreshold slope (SS) caused by poorer short channel effects (SCE) represents a significant limitation for L_{eff} shorter than approximately 15 nm. Decreasing the gate oxide thickness (T_{ox}) to provide better channel control comes with a penalty of increased gate leakage current (I_{gate}) and increased channel doping (to increase threshold voltage, V_T) to maintain I_{off}. Increased channel doping decreases mobility (degrading performance due to impurity scattering), as well as increasing random dopant fluctuations (RDF). Increasing RDF increases variation in V_T with subsequent impact to the minimum operating voltage (V_{min}).

Reducing gate pitch is also a critical challenge for advanced technology generations. Decreasing gate pitch decreases the stress enhancement for both NMOS (stress induced by overlayer films) and PMOS (stress induced by embedded-SiGe, e-SiGe) thus decreasing mobility and drive. Decreasing gate pitch increases the parasitic capacitance contribution for both contact-to-gate and epi-to-gate thus increasing overall gate capacitance (C_{gs}). Finally, decreasing the source/drain opening size increases the source drain resistance (R_{sd}) thus decreasing drive current.

Targeting V_T is a critical challenge for advanced technology generations, particularly for the low power system-on-chip (SOC) processes. The critical conflict is between the need for higher V_T (to produce lower I_{off} and reduce stand-by power) and the need for lower V_T (to produce lower V_{min} and reduce active power).

2. Improving electrostatic confinement

Maintaining the scaling roadmap will require continual improvement in short channel properties. A variety of device architectures which improve electrostatic confinement (and thus short channel control) are being investigated for advanced technology nodes. These architectures can be broadly categorized by the method of electrostatic confinement. There are architectures which provide additional electrostatic confinement with a planar architecture (ultra-thin body (UTB), fully-depleted SOI (FDSOI), extremely thin SOI (ETSOI) etc.), those which use 1′D electrostatic confinement (double gate, FinFET, etc.), those with more than 1′D, but less than 2′D (Trigate, Omega-FET, etc.) and those with full 2′D confinement (gate-all-around (GAA), nanowire etc.) [1]. Electrostatic performance of recent devices is summarized in Table 1.

2.1. Additional electrostatic confinement in planar

The value of fully-depleted UTB SOI for planar electrostatic confinement (as well as the requirements for extremely Si thin layers

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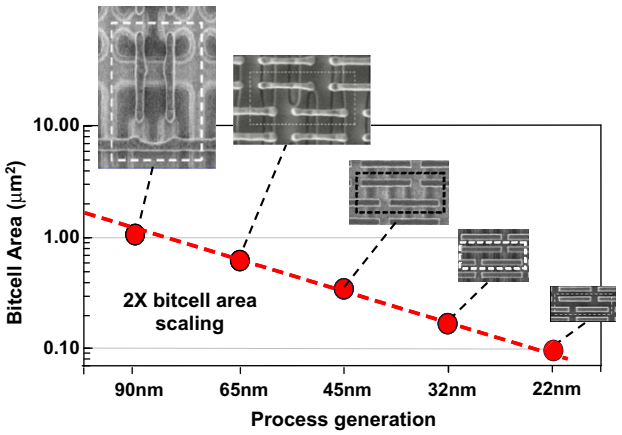

Fig. 1. Steady adherence to Moore's Law has delivered 2X bitcell area scaling each generation.

to achieve well-designed fully-depleted devices) has been recognized since the mid-1980s [2,3]. There has been a steady reduction in the minimum demonstrated body thicknesses (T_{si}) moving from ~100 nm in the 1980s and early 90s [4–6], down to the 15–20 nm range in early 2000 [7–9], and more recently to values significantly below 10 nm [10–16].

UTB SOI devices benefit from using similar manufacturing to planar SOI technology, but with improved SCE, potential for improved RDF (due to lower channel doping) and the possibility for body bias (with thin BOX).

The potential for body-bias in UTB SOI devices [16] is noteworthy. Body-bias is of great interest to the design community (particularly to the SOC design community) to permit active management of V_T in circuit design. However, in conventional planar devices, body bias decreases dramatically as L_{eff} decreases [17] and in 2′D and 3′D devices, there is negligible body bias. In contrast, UTB SOI has significant body bias [16] as well as limited sensitivity of the body effect to L_{eff}. This may offer significant benefit to designers, particularly in the SOC product space.

The potential for improved random variation with UTB SOI devices is also noteworthy. While all the undoped fully depleted devices (UTB SOI, FinFET, GAA) have the potential for low random variation due to undoped channels, in practice the lowest measured random V_T variation values are usually from UTB SOI devices [18].

Challenges of UTB SOI include thin T_{si} effects (external resistance, R_{ext}, scattering, and quantum confinement changes in V_T), difficulties in inducing strain, and manufacturing challenges with the thin T_{si}.

2.2. 1′D and 1′D + confinement

There is a tradeoff between the electrostatic improvement of a GAA device and the fabrication complexity of making gates on all sides of a channel. A number of intermediate architectures (sometimes called multiple gate FET devices or MuGFETs) have been developed in an attempt to get the best SCE with the minimum process complexity [19–39].

Double-gate devices first appeared in the literature in the mid-1980s [19], and a variety of different geometries were explored in the next two decades [20–39]. Variants of the basic device include:

FinFET: Combines double-gate and vertical device concepts for a more manufacturable version of a double gate device [27].

Trigate: Differs from FinFETs in the absence of a gate-blocking layer on the top of the gate. Trigate devices have gates around three sides of the device, providing improved SCE with reduced vertical topography requirements [28,29].

Pi-gates: Differs from Trigates in having the gate extend below the channel. This creates a virtual back gate which shields the back of the channel from electric field lines from the drain, providing improved SCE [30].

Omega-FETS: Differ from Trigates in that the gate not only wraps around three sides, but under-laps part of the fourth. This has an effect similar to Pi-gate in shielding the back of the channel from field lines, resulting in improved SCE [31].

These multiple-gate devices have similar DIBL and RDF advantages over planar as UTB SOI. In addition, the increased confinement in comparison with UTB devices relaxes the manufacturing constraints ($W_{si} \sim 2T_{si}$). Furthermore, tying the gates together provides nearly ideal subthreshold slope. Note also that independent gate operation is possible in some of these architectures.

MuGFETs share the strain and R_{ext} challenges of UTB devices. In addition, these devices face challenges posed by the vertical topography, tight diffusion pitches and complex gate patterning.

2.3. 2′D confinement

GAA devices were first reported in the late 1990s [40–44]. GAA devices differ from Omega-FETs in that the gate wraps entirely around the device. Note that both lateral [40,42], and vertical [41,43], devices are possible with this architecture. Both types provide full two dimensional confinement with the associated SCE benefits.

GAA devices offer the best potential solution to electrostatic confinement challenges. However, these devices face significant challenges. Not only do they have the strain, R_{ext}, vertical topography, tight pitch, and complex gate patterning challenges of the MuGFET devices, but also they face new challenges with gate conformality and excess parasitic capacitance.

Nanowires are an extreme case of GAA devices, having height and width dimensions roughly the same (or even cylindrical) and small (<10 nm) dimensions (Fig. 2, [45–51]). Nanowires add the challenges of phonon scattering [52], (along with possible benefits due to reduction in interface scattering [53,54]).

3. Mobility enhancements

Maintaining the scaling roadmap will require continual improvement in channel mobility. Short term approaches include

Table 1
Comparison of recent results for electrostatic confinement in UTB SOI, fins and wires.

Refs.	Cheng VLSI 2009 [12] ETSOI	Cheng IEDM 2009 [13] ETSOI	Chang IEDM 2009 [37] FIN	Yeh IEDM 2010 [39] FIN	Dupre IEDM 2008 [47] WIRE	Bangsaruntip IEDM 2009 [49] WIRE	Tachi IEDM 2010 [51] WIRE
Gate length	25	25	25	30	90	25/35	32/42
NMOS SS (mV/dec)	85	80	83	75	68	85	64
NMOS DIBL (mV/V)	90	75	83	55	15	65	32
NMOS SS (mV/dec)	80	80	96	74	65	85	73
NMOS DIBL (mV/V)	85	95	158	68	7	105	63