Microelectronic Engineering 88 (2011) 1129–1132

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Accurate analysis of parasitic current overshoot during forming operation in RRAMs

S. Tirano [a,b,*], L. Perniola [a], J. Buckley [a], J. Cluzel [a], V. Jousseaume [a], Ch. Muller [b], D. Deleruyelle [b], B. De Salvo [a], G. Reimbold [a]

[a] CEA-LETI, MINATEC Campus, 17 rue des Martyrs, F-38054 Grenoble, France
[b] IM2NP, UMR CNRS 6242, Aix-Marseille Université, F-13451 Marseille Cedex 20, France

ARTICLE INFO

Article history:
Available online 6 April 2011

Keywords:
Resistive switching memory
Current overshoot
Electroforming
Parasitic capacitance
Memory operations

ABSTRACT

In this paper, a peculiar attention is turned towards the understanding of the current overshoot occurring during the forming operation in resistive switching memory devices. This phenomenon is attributed to the discharge of a parasitic capacitance in parallel to the resistive device in simple 1R (one resistor, no transistor/diode selector) architectures. The impact of such an overshoot is analyzed on both NiO and HfO_2-based memory elements by performing measurements with different setups (quasi-static and pulse measurements). We show that the parasitic event is more severe as the forming voltage in the memory device increases. Moreover, it is shown that the post-forming resistance cannot be simply adjusted by a current compliance available on semiconductor parameter analyzers, since this internal limiter is ineffective in the microsecond range for compliance levels lower than the current spike. The current overshoot playing a detrimental role on the electrical performances of resistive devices, it must be carefully monitored when assessing the electrical performances in simple 1R architectures.

1. Introduction

Resistive Random Access Memory (RRAM) is a new attractive non-volatile memory technology offering high potential in terms of integration density, low power consumption, high-speed operations and ease of fabrication [1]. Typically RRAMs can exhibit large ON/OFF ratio (>10^6) [2] and switching time in the nanosecond range [3]. Such large and fast resistance swing during forming/set operation induces a current overshoot during transition that the compliance of the semiconductor parameter analyzer (SPA) is not able to limit instantly. Understanding and controlling this parasitic phenomenon is required for reliable electrical operations in such memories. Even if the presence of this parasitic event during the switching of simple 1R (one resistor without selector device) devices has been already mentioned [4], no dedicated quantitative analysis has been reported so far in literature. Hence, this paper presents, for the first time, a detailed analysis of current overshoot during forming operation in analytical RRAM devices.

2. Device fabrication

Fig. 1 shows the scheme of typical analyzed capacitor-like RRAM structures: they are composed of two 25 nm thick Pt sputtered electrodes sandwiching NiO or HfO_2 resistive switching layer with thicknesses ranging from 10 to 20 nm. For NiO-based devices, the nickel oxide layer was formed by thermal oxidation of a thin Ni layer deposited by PVD (Physical Vapor Deposition) and annealed under oxygen flow at 450 °C [5]. In contrast, for HfO_2-based devices, the hafnium oxide layer was deposited at 350 °C by ALD (Atomic Layer Deposition) using $HfCl_4$ and H_2O as precursors. Area memory elements (2.54 μm^2) were patterned by IBE (Ion Beam Etching) monitored by SIMS (Secondary Ion Mass Spectrometry) [2].

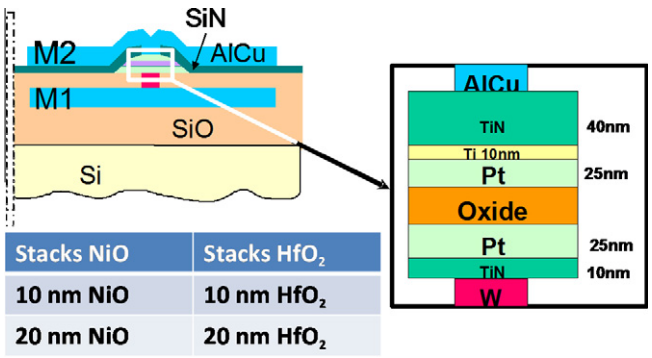
3. Transient electrical behavior

3.1. Forming electrical characteristics

Current–voltage *I–V* characteristics were measured during the forming operation with either a standard parameter analyzer HP 4155 or a pulse generator KI 3402 that enabled varying voltage ramps from 0.1 to 10^6 V/s. Fig. 2 shows typical *I–V* curves measured on NiO and HfO_2-based cells with a voltage ramp of 0.1 V/s on a standard SPA. It is shown that the resistance in pristine state is significantly larger for HfO_2-based cells with respect to NiO-based cells (i.e. $R \sim 10^{12}\ \Omega$ @ 50 mV for HfO_2 against $R \sim 10^8\ \Omega$ @ 50 mV for NiO). In complement, Weibull plots measured on few tens of memory elements showed that the forming voltage is significantly larger for HfO_2-based cells and increases along with thickness (not shown here). Finally, Fig. 3 demonstrates a monotonic increase of the forming voltage over the investigated range of voltage ramps.

* Corresponding author at: CEA-LETI, MINATEC Campus, 17 rue des Martyrs, F-38054 Grenoble, France.
E-mail address: sauveur.tirano@cea.fr (S. Tirano).

0167-9317/$ - see front matter © 2011 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2011.03.062



Stacks NiO	Stacks HfO_2
10 nm NiO	10 nm HfO_2
20 nm NiO	20 nm HfO_2

Fig. 1. Schematic of the capacitor-like resistive memory structures. The test devices are in simple 1R configuration (i.e. no series selector fabricated next to the device).

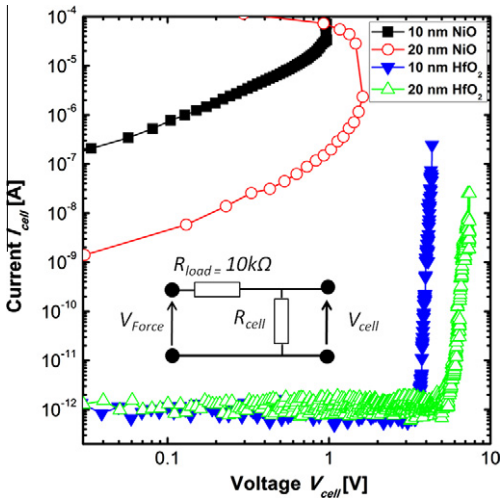


Fig. 2. Forming operation measured in quasi-static mode with a HP 4155 SPA on HfO_2 and NiO-based memory devices. Typical *I–V* characteristics measured under a voltage ramp force of 0.1 V/s (each characteristic is the average of 20 devices).

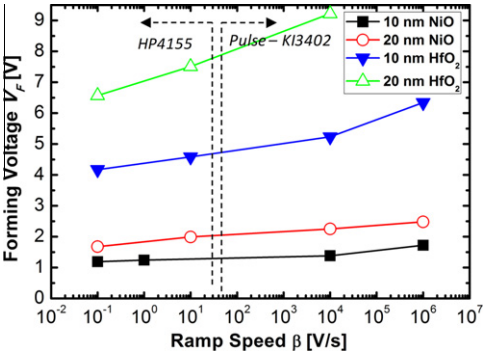


Fig. 3. Ramp speed dependent evolution of forming voltages. Measurements were performed by using either quasi-static (SPA) or pulse modes to reach a large range of ramp speeds.

3.2. Analysis of current overshoot during forming operation

To understand the non-equilibrium processes during transition, an accurate study of current passing through the cell during the forming process was performed using the setup depicted in Fig. 4a. The current flowing through the device was measured across a resistor (R_{read}) placed between the cell and the ground whereas a load resistor R_{load} of 10 kΩ placed between the SPA and the cell was used as a current limiter. Traditional setup without load resistor (R_{load} being shunted) was also used to evaluate the efficiency of the SPA current compliance regulator. Fig. 5 shows that the current overshoot in time directly depends on the amplitude of the forming voltage: the larger the forming voltage, the larger the amplitude and duration of the overshoot are. Besides, it has to be noted that in principle it should not go beyond the SPA compliance fixed in this case at 1 mA. However, in the case of 20 nm thick HfO_2 layer, the current spike exceeds 50 mA after 0.5 µs and is damped only after 30 µs thanks to the SPA compliance. This can be explained by the limited slew rate of about 0.2 V/µs in SMU (Source Measure Unit) connected to SPA, while the resistance switching toward ON state occurs in the range of few ns. For smaller V_F, as for 20 nm thick NiO layer, the current overshoot is limited to 3 mA during the first µs. As shown in Fig. 6 for 10 and 20 nm thick HfO_2 layers, the current compliance modifies the post-forming resistance. Indeed, for a current compliance in the range 50 µA–10 mA, the resistance in ON state is around 100 Ω while it decreases to few ohms for current compliances larger than 10 mA. The same trend has been reported by Kinoshita et al. for the set operation in NiO-based memory elements [6]. This typical behavior may be satisfactorily explained by a forming mechanism based on a local redox process [7]: in that case, the current compliance enables controlling the diameter of the conductive filaments created within the oxide layer and subsequently adjusting the resistance level in the conductive state. However, on the experimental point-of-view, the present results suggest that the SPA compliance is ineffective to reach a specified resistance level. As a consequence, a dedicated current limiter must be integrated into the device to remove the current overshoot, such as a transistor in series to the resistive capacitor-like structure in 1T/1R memory cells [8]. By introducing a load resistance R_{load} = 10 kΩ in the circuit, the current spike associated with the regulator delay is removed (Fig. 7) since the voltage drop on the resistive element is transferred to R_{load} during forming. The load resistance physically limits the current $I_{max} = V_{Force}/(R_{load} + R_{cell} + R_{read})$ but does not remove the residual transient over-current appearing during switching and corresponding to the transfer of the voltage drop from the device to the load resistor. As proposed by Ielmini et al. on NiO-based RRAM elements for the set operation [9], the residual overcurrent during forming operation may be attributed to the discharge of the parasitic capacitance toward the resistive memory element (Fig. 4b). The transient current flowing through the cell is:

$$i(t) \approx \frac{V_{\mathrm{Force}}}{R_{\mathrm{load}} + R_{\mathrm{Cell}} + R_{\mathrm{read}}} + \frac{V_{\mathrm{Force}} - V_{\mathrm{Rload}}}{R_{\mathrm{Cell}} + R_{\mathrm{read}}} \exp\left[-\frac{t}{(R_{\mathrm{Cell}} + R_{\mathrm{read}}) \cdot C_{\mathrm{p}}}\right] \quad (1)$$

C_p being the overall system capacitance due to the built-in capacitance of the fabricated device plus the capacitance of the measurement setup. The post-forming resistances in quasi-static measurements for HfO_2-based cells with a load resistance are similar to those obtained with a current compliance on SPA. This result implies that post-forming resistance is mainly defined during the very first nanoseconds where stands the initial residual overcurrent.

3.3. Forming operation with high frequency pulses

For the forming operation using a pulse-mode measurement, attention was paid on 10 nm thick HfO_2 layer for which the