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Three-interface pseudo-MOSFET models for the characterization of SOI wafers with ultrathin film and BOX

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ABSTRACT

The electrical characterization of unprocessed fully depleted silicon-on-insulator (SOI) layers relies on the pseudo-MOSFET (Ψ-MOSFET) technique. We propose three-interface models which are more appropriate for addressing the case of SOI wafers with ultrathin body and BOX (UTB^2). The novel models for threshold voltage and subthreshold swing account for the channel-to-surface and channel-to-substrate coupling which are important effects, respectively, in ultrathin films and thin BOX. The influence of the density of traps at each of the three interfaces (free surface, channel/BOX and BOX/substrate) is discussed. The models are validated with experimental results from a range of SOI film thicknesses.

1. Introduction

SOI wafers are evolving to nanosize layers needed for aggressive scaling. Fully depleted (FD) structures with ultrathin body and ultrathin buried oxide (BOX) enhance the electrostatic integrity of short channel devices. These SOI wafers are suitable for high speed, low-power and DRAM applications.

The electrical characterization of FD layers is very difficult unless applying a substrate bias. In this context, the Ψ-MOSFET technique, which uses the intrinsic upside-down MOS structure in SOI (Fig. 1) is successful as it enables wafer monitoring before device processing [1,2]. The classical Ψ-MOSFET model [2] simply accounts for the film-BOX interface (I_1) where the carriers flow. We have recently proposed a two-interface model which depicts the case of ultrathin Si films [3]; the properties of the top surface (I_2), passivated or non-passivated, impact the channel electrostatics and carrier transport [4]. In this paper, we extend the model for very thin BOX, where the quality of the BOX-substrate interface (I_3) and the energy-bands bending in the substrate (Fig. 2) can also affect the channel properties.

Fig. 3.a shows the evolution of the threshold voltage as a function of the BOX thickness obtained from numerical solution of Poisson equation when the silicon substrate underneath the BOX is considered. As the BOX is thinned down below 50 nm, the role of the substrate starts to be noticeable. The electrostatic potential drop at the substrate-BOX interface (Fig. 2) becomes comparable with the threshold voltage, leading to characterization errors. Fig. 3b shows the relative error in threshold voltage evaluation when the same simulation as in Fig. 3a is performed by considering that the gate voltage is applied directly at the BOX-substrate interface (i.e. neglecting the substrate effect). For non-passivated samples, the role of the substrate can be ignored for BOX thickness above 80 nm (error <10%), because the main contribution is due to the free surface. However in passivated samples, the inclusion of the substrate in the models is crucial since even in a standard 145 nm-thick BOX wafer the error may reach an unacceptable value of 20%. Such errors lead to disproportionate overestimate of the trap density at film-BOX interface.

2. Three-interface models

The gate voltage supplied to create the channel relates to the potential drop in the silicon film ($q\psi_{S1} = E_F(0) - E_{Fi}(0)$), buried oxide ($\psi_{BOX} = E_{BOX} \cdot t_{BOX}$) and substrate ($q\psi_{S3} = E_F(-t_{BOX}) - E_{Fi}(-t_{BOX})$):

$$V_G = \phi_{fb} + \psi_{S1} + \psi_{BOX} - \psi_{S3} \quad (1)$$

where ϕ_{fb} is the workfunction difference between the film and the substrate. ψ_{S1} is governed by the density of traps at the buried and top interfaces (D_{it1}, D_{it2}) and ψ_{S3} accounts for the energy-bands bending within the substrate. Its role is similar to the poly-depletion effect in conventional MOSFETs [5]. Assuming that the BOX is

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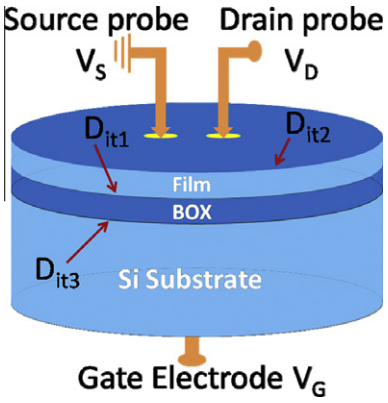

Fig. 1. Schematics of the pseudo-MOSFET transistor.

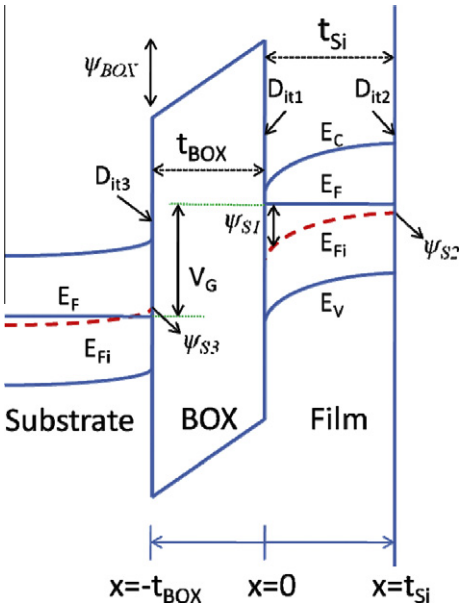

Fig. 2. Three-interface energy-bands diagram for pseudo-MOSFET with electron channel ($V_G > 0$).

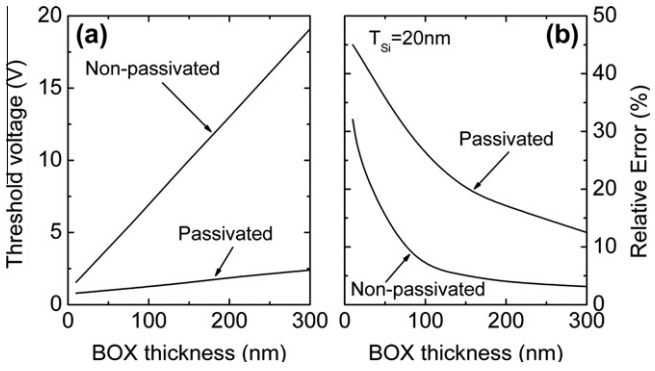

Fig. 3. (a) Simulated threshold voltage evolution as a function of the BOX thickness in a 20 nm thick Ψ-MOSFET with passivated ($D_{it2} = 2 \times 10^{11}$ cm^{-2} eV^{-1}) and non-passivated ($D_{it2} = 2 \times 10^{13}$ cm^{-2} eV^{-1}) free surface and $D_{it1} = D_{it3} = 2 \times 10^{11}$ cm^{-2} eV^{-1}. (b) Relative error in threshold voltage between simulations with two-interfaces (neglecting substrate effects) and three-interfaces.

free of internal charge, the following relation between the surface potentials holds (see Fig. 2):

$$-\epsilon_{Si}\left(\frac{d\psi}{dx}\right)_{x=-t_{BOX}} - qD_{it3}\psi_{S3} = \epsilon_{OX}E_{BOX} = qD_{it1}\psi_{S1} - \epsilon_{Si}\left(\frac{d\psi}{dx}\right)_{x=0} \quad (2)$$

where an uniform distribution of traps within the gap energy has been considered for achieving tractable expressions.

The solution of Eq. (2) for different interface cases is computed in Fig. 4. For equal interface quality (low density of interface states: $D_{it1} = D_{it3} = 2 \times 10^{11}$ cm^{-2} eV^{-1}), the gate bias first serves to adjust the depletion and accumulation of the substrate underneath the BOX; only when ψ_{S3} reaches $-2\phi_F$ ($\sim$−460 mV) the inversion channel starts to form and ψ_{S1} increases rapidly. If the density of states at the substrate-BOX interface is high, the potential ψ_{S3} becomes pinned with limited variation. In the unrealistic case of a very degraded bonded interface I_3 ($D_{it3} = 2 \times 10^{13}$ cm^{-2} eV^{-1}), the substrate interface is never accumulated before the onset of the inversion channel.

The following two approaches can be used for modelling.

2.1. Analytic model

The surface potentials at the channel/BOX and BOX/substrate interfaces can be inter-related through Eq. (2): $\psi_{S3} = -\lambda\psi_{S1}$. The coupling factor λ, solution of Eq. (2), is shown in Fig. 5 at threshold for different wafer parameters.

In the majority of realistic cases (small D_{it3}), Eq. (2) does not need to be solved and the coupling factor can be approximated by the following values: $\lambda \sim 1.1$ for the case of non-passivated wafers; $\lambda \sim 1.03$–$0.67 \log(D_{it3}/2 \times 10^{11})$ for passivated wafers. The threshold voltage can be derived by applying Gauss' law to the transistor body and combining with Eqs. (1) and (2). Considering the approximation of $\psi_{S1} = 2\phi_f$ at threshold, V_T is given by:

$$V_T = \phi_{fb} + 2\phi_F\left(1 + \lambda + \frac{C_{it1}}{C_{Box}} + \frac{C_{Si}C_{it2}}{C_{Box}(C_{Si} + C_{it2})}\right) \quad (3)$$

where $C_{it1} = qD_{ti1}$, $C_{it2} = qD_{ti2}$.

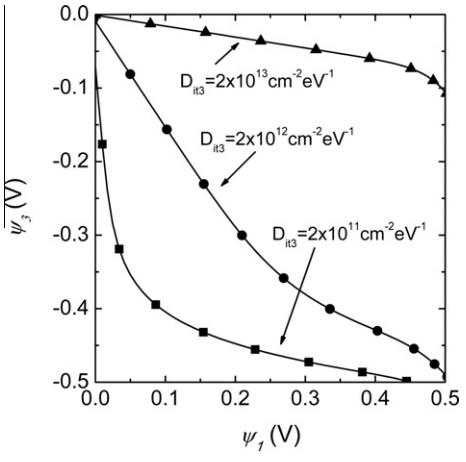

Fig. 4. Electrostatic potential at the substrate/BOX interface, ψ_{S3}, as a function of the buried channel potential, ψ_{S1}, for different densities of traps at the substrate/BOX interface. The solid lines corresponds to a BOX thickness of $T_{BOX} = 145$ nm, whereas the results in symbols to $T_{BOX} = 10$ nm. $T_{Si} = 20$ nm, $D_{it1} = 2 \times 10^{11}$ cm^{-2} eV^{-1}, $D_{it2} = 2 \times 10^{13}$ cm^{-2} eV^{-1} (non-passivated wafer showing potential pinning at the surface), $N_{A\text{-film}} = N_{A\text{-sub}} = 10^{14}$ cm^{-3}.