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Ultrathin EOT high-κ/metal gate devices for future technologies: Challenges, achievements and perspectives (invited)

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ABSTRACT

Ultrathin EOT-values are achieved by using optimized processing conditions and interface layer scavenging in metal-gated (TiN and TaN) HfO_2 based planar and bulk-FinFET devices. EOT values down to 4.5 Å ($T_{inv} \sim 8.5$ Å) in the planar devices and $T_{inv} < 11$ Å in bulk-FinFETs are demonstrated. Improved EOT-leakage current scaling is observed with the use of chemical oxides as compared to thermally grown SiO_2 as interface layer for the HfO_2. In contrast, the mobility is found independent of the compared interface layers, processing conditions and metal electrodes and follows one trend-line with EOT. The FinFET devices show decreased T_{inv}-values and improved mobility for more narrow fin widths.

1. Introduction

The gate-stack optimization efforts over the past years have more recently resulted in the successful implementation of ultrathin (UT) EOT devices (EOT < 5 Å) with excellent *n* and pMOS device performance [1,2]. However, the commonly observed severe mobility degradation from thinning down the SiOx interface layer (IL) [1–3] reduces the EOT-scaling benefits. While there are reports elaborating on the origin of the low mobility at low EOT e.g. [2], there is less done on UT-EOT devices with alternative device architectures e.g. FinFETs [4] or fully depleted (FD) SOI [5] and channel materials e.g. Si_xGe_{1-x} [6,7] or III–V materials [8]. In a previous study [9] the impact from EOT scaling on ultrathin BOX (UTBOX) ultrathin-body fully depleted SOI (FDSOI) and SiGe quantum wells (QW) were compared to that of Si planar devices. In this paper, the comparison is extended to ultrathin EOT Si based bulk finfet devices (BFF) [4] with fin widths down to ~25 nm.

1.1. Device fabrication

Planar and bulk FinFET MOS devices were fabricated on 300 mm ⟨100⟩ Si wafers using a gate-first metal inserted poly-Si process (MIPS) [1,6]. The high-κ dielectric HfO_2 was deposited by ALD at 300 °C from $HfCl_4$ and H_2O precursors on a variety of SiO_2 interface layers (IL) as shown in Table 1.

The chemical oxide (from imec-clean) was grown at room temperature in a de-ionized H_2O bath with 1 ppm of O_3 for 1 min. The thickness of the chemical oxide is self-limiting, while the ISSG and thermally grown oxide thicknesses were controlled by temperature and time. To achieve a thin high quality thermally grown oxide, a 3-nm-thick SiO_2 layer was grown at 1100 °C and then etched-back in HF to 0.8 or 1.2 nm (Table 1).

Optional La cap layer for V_T tuning and the metal electrode with a Si-cap were deposited in situ [1] by means of PVD. Two metals are compared in this study, TiN and TaN, both with an approximate 1:1 composition [10]. The thickness of the metal layers is between 2 and 10 nm as estimated by X-ray reflectometry (XRR) and high resolution transmission electron microscopy (HRTEM). Prior to metal deposition, and to control interfacial growth [11], the HfO_2 was degassed at 350 °C for 4 min.

The Si-cap was etched in HF to remove any formed native oxide immediately followed by poly-Si deposition and standard processing to etch the gate-stack, implant extensions and halo's, deposit spacers and define HDD's. The standard activation anneal for the studied devices was a 1035 °C spike anneal, but in a few cases was a laser-anneal (LA) used. The devices were processed until the first metal level.

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Table 1
The various interfacial oxides with growth conditions compared in this study.

	imec-clean chem. oxide	ISSG	SiO_2 (EB)
Temperature	Room-T	760–900 °C	1100 °C
Ambient	DIW (O_3)	N_2O/H_2	O_2
Thickness	0.9 nm	0.8, 1.2 nm	0.8, 1.2 nm
Thickness-control	Self-limiting	Temperature/time	Etch-back

1.2. Electrical characterization

Capacitance–Voltage (C–V) measurements were done with an Agilent 4284A multi-frequency LCR meter at frequencies between 100 kHz and 1 MHz on capacitors with area ranging from 900 to 3600 μm^2 and 10 × 10 μm^2 transistors. Additionally, higher frequency measurements (up to 50 MHz) were carried out with an Agilent 4294A impedance analyzer with impedance matching probe 42941A. Dedicated RFCV structures and ground-signal-ground probes were used for optimum series resistance and parasitic control [12] to enable accurate C—V measurements for devices with high leakage currents. The EOT was obtained by fitting of the C—V traces with the CVC tool [13].

The inversion capacitance equivalent thickness (T_{inv}) was calculated from the capacitance in inversion (C_{gc}) at offset from V_T as $T_{inv} = C_{gc}(V_g = V_T + 0.6\ V)$. The T_{inv} and EOT follow the approximate relation $T_{inv} \sim EOT + 4$ Å. The effective inversion channel electron mobility (μ_{eff}) and effective electric field (E_{eff}) were calculated with the split C–V technique [14,15] with linear drain–source currents (I_D) measured with a Keithley 4200 at a drain voltage ($V_{D,lin}$) of 50 mV on long channel devices (W = 10 μm, L = 1–10 μm). The inversion charge was averaged between the source and drain to take the gate-leakage and non-zero drain voltage into account [15].

For FinFETs, the electrical thickness in inversion was extracted from

$$T_{inv} = \frac{C_{gc}|_{V_G=V_T+0.6\ V}}{(W_{fin} + 2H_{fin})L}\frac{1}{\varepsilon_{SiO_2}} \quad (1)$$

where the physical fin width (W_{fin}) and height (H_{fin}) were estimated from HRTEM images. Note that while T_{inv} is sensitive to small errors in W_{fin} and H_{fin}, the mobility is only dependent on the drain current (I_{ds}), inversion channel capacitance (C_{gc}) and channel length (L) according to [16]:

$$\mu(V_g) = \frac{I_{ds}(V_g)L}{V_{ds}W}\frac{1}{qN_s} = \frac{I_{ds}}{V_{ds}}\frac{L^2}{q\int_{V_G<V_T}^{V_G} C_{gc}dV_g} \quad (2)$$

where q is the elementary charge, $W = N_{fin}(W_{fin} + 2H_{fin})$ is the total fin width (N_{fin} is the number of fins) and N_s is the inversion charge density from C_{gc}:

$$qN_s(V_g) = \int \frac{C_{gc}}{WL}dV_g. \quad (3)$$

In long channel devices (here $L = 10$ μm) δL can be assumed negligible and the effect from series resistance is negligible in contrast to the mobility extraction in short channel FinFETs [17].

2. Results – achieving ultrathin EOT

2.1. Metal electrodes and cap dielectrics

Choosing the metal electrode is of critical importance to achieve ultrathin EOT values. Shown in Fig. 1a is a comparison in EOT-scaling between TaN and TiN as function of the metal-gate (MG) thickness. For both metals is a strong reduction in EOT observed as the thickness of the metal is scaled down. However for TiN the values are considerably lower and the trend with MG-thickness is steeper.

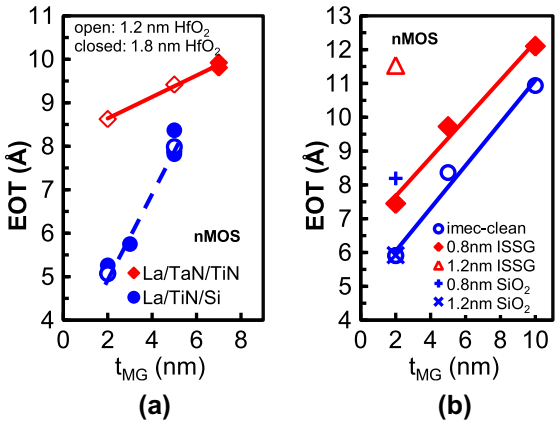

Fig. 1. 1a EOT extracted from C to V measurements on nMOS capacitors with imec-clean HfO_2/La/MG/2 nm Si as function of the MG thickness for TiN and TaN. Thinner MG results in lower EOT. 1b EOT as function of TiN thickness for 1.8 nm HfO_2/2—10 nm TiN/2 nm Si on various starting interface layers. The EOT is thinner with imec-clean as compared to ISSG. Similar results are found for pMOS.

The EOT-scaling is also determined by the quality and thickness of the starting IL. Fig. 1b shows improved EOT scaling with imec-clean (chemical oxide) over 0.8 nm ISSG by about 1.5 Å. A thicker ISSG (1.2 nm) results in further increase in EOT while the thermally grown SiO_2 with etch-back is close to identical to imec-clean.

Fig. 1 also shows the improved EOT-scaling with La-capping. The data in Fig. 1a is with La-cap while Fig. 1b is without La. The EOT with La-cap is approximately 1 Å thinner. This is in good agreement with other studies [18].

The leakage current scales with EOT similarly for the two metals as shown in Fig. 2a with lower J_G values at higher EOT for the TaN. Thinner HfO_2 results in higher J_G values as expected. The J_G is on the other hand quite different for the different interface layers (Fig. 2b). The leakage current for the gate-stack grown on the imec-clean chemical oxide is ~20 times lower at a given EOT, or equivalently the EOT is 2 Å lower at a given J_G. Similar results are observed for n and pMOS.

Ultrathin EOT relies on achieving thin or non-existing interface layers. The EOT contribution of the HfO_2 is 2–4 Å for 1.2–2.0 nm HfO_2 assuming a κ-value of 20. To achieve EOT values at or below 5 Å the interface therefore must be below 3 Å. Shown in Fig 3a–c are HRTEM images of gate-stacks with 5 nm TaN, 5 nm TiN and 2 nm TiN, respectively which were deposited on imec-clean/1.8 nm HfO_2. In the TaN case a clear interface layer of ~1.3 nm is observed. The IL is thinner for 5 nm TiN (~0.9 nm) and in the 2 nm TiN case, the IL is barely visible (<0.2 nm). The ultrathin EOT values for thin TiN shown in Figs. 1 and 2, hence correlates well with a reduction of the interfacial SiO_2 thickness.

2.2. Process timing

Moisture control in HfO_2 and its impact on EOT-scaling in TaN gated devices was previously studied in detail [11]. Thinner EOTs were obtained by degassing of the HfO_2 prior to metal deposition. The origin of the improvement was found to be related to less re-oxidation of the interface during the high thermal budget steps resulting from removal of H_2O from the bulk of the HfO_2 as well as surface bound OH-groups.

The observed improvement in EOT-scaling with TiN and La-cap can be explained by the SiO_2 scavenging reactions by Ti and La [18]. However, even in this case the processing condition is of importance. Shown in Fig. 4 are gate-leakage current values as