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SiON and SiO_2/HfSiON gate oxides time dependent dielectric breakdown measurements at nanoscale in ultra high vacuum

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ABSTRACT

Time dependent dielectric breakdown (TDDB) measurements on a nano-scale using an AFM tip under ultra high vacuum as upper electrode are systematically compared to device measurements in this paper. Both studies were performed on the same SiON or SiO_2/HfSiON gate oxides. The shape factor of the TDDB distribution and the acceleration factor are compared at both scales.

1. Introduction

Atomic Force Microscopy in Conduction mode (C-AFM) is widely used for current–voltage measurements allowing electrical characterization at nanometric scale [1,2]. C-AFM electrical characterization has a strong industrial interest since it allows in principle to avoid costly technological steps (electrode deposition, patterning) at least for gate oxide monitoring. However, the contact area between the AFM tip and the dielectric is unknown and not well controlled in atmospheric condition because of water and organic contamination. Moreover, the link between electrical characteristics made with C-AFM and on standard devices has to be established. Recently, nanoscale electrical characterization has been performed to determine the cumulative failure distribution of TDDB [3] with a C-AFM operating at 10^{-6} torr. Although consistent values of the Weibull β-slopes at nanoscale and at devices measurements were established, the voltage dependence and the surface scaling were not discussed. More recently, the lifetime extrapolations were shown to be difficult to compare with their counterparts made on standard devices [4]. The aim of this paper is to compare systematically gate oxide TDDB distributions obtained on standard MOS structures and on unpatterned SiON or SiO_2/HfSiON layers by C-AFM in ultra high vacuum (UHV) 10^{-9} torr environment.

2. Experimental

In the present study, tests were carried out on a 2.6 nm thick SiON layer and on a SiO_2/HfSiON stack on Si (5.07×10^{15} cm^{-3}, p type). The SiON layers investigated in this study were formed by performing a pulsed RF decoupled plasma nitration process. The SiO_2 base layer was formed by thermal oxidation at 980 °C in O_2 flow. Finally, samples were annealed at 1100 °C under O_2 flow to stabilize N atoms in the oxide. The HfSiON bilayer was obtained by plasma nitration of a SiO_2 (8 Å)/HfSiO (17 Å) stack. C-AFM measurements were performed at room temperature (23 °C) with an Omicron AFM/scanning tunnelling microscopy system with a conductive diamond tip (B doped) under UHV (<10^{-9} torr) in order to avoid water and organic contamination that can lead to drift in the onset voltage [2] and anodic oxidation. The AFM tip served as a top electrode and voltage was applied to it. The substrate was grounded. The current was recorded by a Keithley 6430 electrometer equipped with a sub-femtoamper sourcemeter. Electrical contact between sample and stage was assured with indium solder, and all the samples were outgased at 150 °C for 3 h at 4×10^{-8} torr. Current measurements were carried out with a normal force of 20 nN. All the C-AFM measurements have been performed with the same tip. For each voltage a minimum of 40

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current versus time $I(t)$ measurements were recorded. Device measurements were done with a HP4156 Semiconductor parameters analyzer at 125 °C on NMOS transistors with surfaces from 0.04 to 4 μm^2. Oxide layers for device measurements and nanoscopic measurements have been obtained within the same process flow. A Polysilicon N + gate (5×10^{19} cm^{-3} As doped) was then deposited only for devices measurement samples. For the nanoscopic sample we use the AFM tip as the gate electrode.

Fig. 1 shows a topographic image (1×1 μm^2) of a 2.6 nm thick SiON layer after a 4×6 grid of breakdown tests. Bumps in the image (bright spots) corresponds to the location of the $I(t)$ test. Those topographic bumps are due to field induced epitaxy that creates a real change of topography [5]. The resulting $I(t)$ characteristics are compared to NMOS device measurements on a 300 mm wafer. This comparison is illustrated on Fig. 2, where $I(t)$ recorded with C-AFM at 5.2 V together with $I(t)$ recorded on a 0.04 μm^2 NMOS at 3.5 V are plotted. Whatever the surface one observes a sharp increase of the current for both dielectric layers when hard breakdown occurs. The time to breakdown (TBD) detection criterion in this study corresponds to hard breakdown and then current threshold detection. Note that the TBDs from Fig. 2 are in the same range of magnitude despite to the expected surface difference. This is due to the applied voltage (5.2 V with C-AFM vs. 3.2 V on the 0.04 μm^2 transistor gate). Indeed the mean breakdown field is much higher on nanometric samples [6], which allow higher applied voltage than for standard devices. The small tip surface contact area leads to a higher mean time to failure (MTTF) due to area scaling, which is compensated by a higher voltage applied for the C-AFM experiment. One can notice the higher noisy aspect of C-AFM $I(t)$ characteristics. In order to achieve a more quantitative comparison, we have plotted two $I(t)$ traces with the same current intensity scale in Fig.3. The initial current measured with C-AFM is lower by more than two decades than the current measured on 0.04 μm^2 transistor. This can be explained by the difference of the tunnelling current for these two areas. A more progressive breakdown and noisy aspect is observed in the case of C-AFM trace. Let's assume that the $I(t)$ is the sum of the tunnelling current proportional to the area and a contribution from the degradation mechanism increasing with time. Decreasing the area leads to a decrease of the tunnelling current that masks the degradation contribution.

On Figs. 4 and 5 we have reported the cumulative failure distribution of TDDB obtained by C-AFM measurements at different tip voltages for SiON and SiO_2/HFSiON gate oxides, respectively. In the first case the distribution in Weibull scale is linear similarly to the

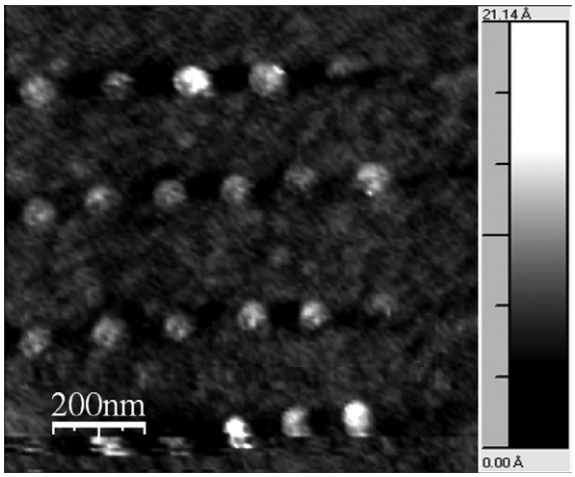

Fig. 1. AFM topography image taken after a 6×4 $I(t)$ grid on a 2.6 nm thick SiON oxide layer on Si substrate.

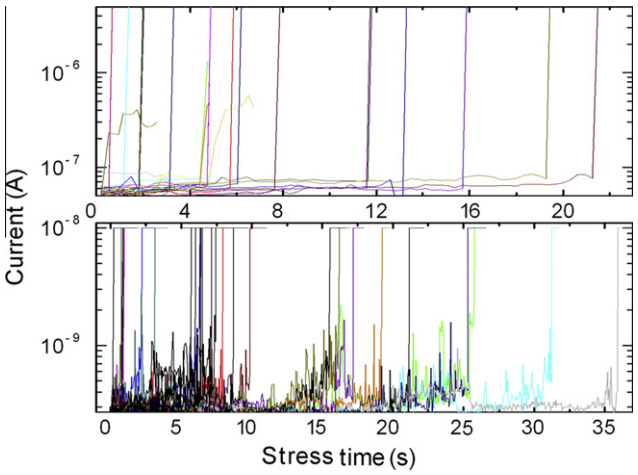

Fig. 2. $I(t)$ traces recorded on a 2.6 nm thick SiON oxide layer on Si substrate with C-AFM at 5.2 V (bottom) and on a 0.04 μm^2 NMOS at 3.5 V (top). A dispersion of the TDDB in both case is observed.

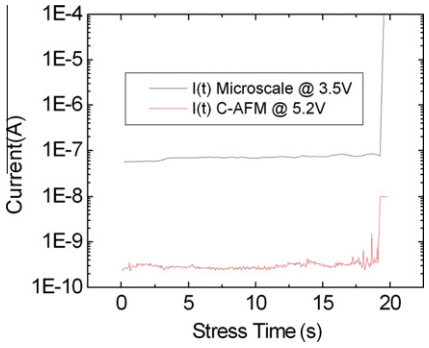

Fig. 3. $I(t)$ traces recorded on a 2.6 nm thick SiON oxide layer on Si substrate with C-AFM at 5.2 V and on a 0.04 μm^2 NMOS at 3.5 V plotted on the same scale.

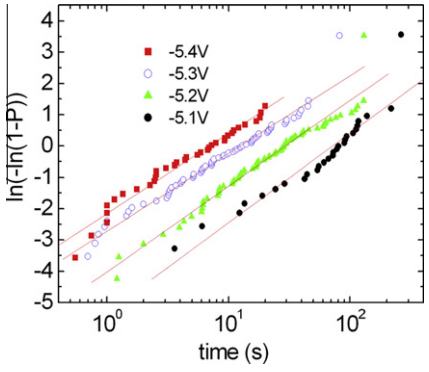

Fig. 4. Cumulative failure distribution obtained by C-AFM on SiON. This distribution was fitted by a unimodal Weibull distribution.

device measurements on NMOS (SiON gate oxide) reported in Fig. 6 for 0.04 and 4 μm^2. This is in contrast with the bimodal distribution observed for the bi-layer sample, similar to the bi-layer dielectric gate stack distribution already reported on standard micrometric devices [7].For a single layer the cumulative Weibull distribution of TDDB is given by [3,4]

$$P(t) = 1 - \exp(-(t/\sigma)^{\beta}) \quad (1)$$

If A_0 is the surface of a unit capacitor and A the surface of the device under test the surface scaling is given by: $(1 - P(t))^{(A/A0)}$). The plot of $\mathrm{Ln}(-\mathrm{Ln}(1 - P(t))$, is a linear function of $\mathrm{Ln}(t)$ (i.e. Weibull scale) for