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Cryogenic single-chip electron spin resonance detector

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ABSTRACT

We report on the design and characterization of a single-chip electron spin resonance detector, operating at a frequency of about 20 GHz and in a temperature range extending at least from 300 K down to 4 K. The detector consists of an LC oscillator formed by a 200 μm diameter single turn aluminum planar coil, a metal–oxide–metal capacitor, and two metal–oxide–semiconductor field effect transistors used as negative resistance network. At 300 K, the oscillator has a frequency noise of 20 Hz/Hz$^{1/2}$ at 100 kHz offset from the 20 GHz carrier. At 4 K, the frequency noise is about 1 Hz/Hz$^{1/2}$ at 10 kHz offset. The spin sensitivity measured with a sample of DPPH is 10^8 spins/Hz$^{1/2}$ at 300 K and down to 10^6 spins/Hz$^{1/2}$ at 4 K.

1. Introduction

Methods based on the electron spin resonance (ESR) phenomenon are used to investigate samples in a wide temperature range, ranging from above 1000 K [1–4] to below 1 K [5,6]. Low temperature measurements are usually performed in large microwave cavities as well as with miniaturized conductive [7,8] or superconducting [9–11] resonators. Miniaturized resonators are typically used to maximize the signal-to-noise ratio in experiments with mass-limited samples [7,12–17]. In Refs. [13,18,19] we presented single-chip integrated inductive ESR detectors, fabricated using complementary metal oxide semiconductor (CMOS) technologies, operating between 8 GHz and 28 GHz. The ESR phenomenon was detected as a variation of the frequency of an integrated LC-oscillator due to an effective variation of its coil impedance caused by the resonant complex susceptibility of the sample. Operation in the temperature range from 300 K to 77 K was demonstrated in Refs. [18,19]. Here, we report on the implementation of a 20 GHz single-chip ESR detector, based on the same operating principle, but capable of operating from 300 K down to at least 4 K. Depending on the specific sample (and, in particular on the dependence of its relaxation times on temperature), the possibility to operate down to 4 K might represent a significant advantage in terms of spin sensitivity (larger polarization, lower thermal noise) as well as in terms of information richness. The fabricated device represents also the first demonstration of a CMOS microwave oscillator operating down to 4 K.

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2. Operating principle

The principle of operation of the realized single-chip ESR detector is identical to that reported in our previous work Refs. [13,18,19]. In typical experimental conditions, the oscillation frequency of an LC-oscillator coupled with an ensemble of electron spins is given by [19]

$$\omega_{LC\chi} \cong \frac{\omega_{LC}}{\sqrt{1+\eta\chi'}} \tag{1}$$

where

$$\chi' = -\frac{1}{2}\frac{(\omega_{LC\chi}-\omega_0)T_2^2}{1+T_2^2(\omega_{LC\chi}-\omega_0)^2+\gamma_e^2B_1^2T_1T_2}\omega_0\chi_0 \tag{2}$$

is the real part of the magnetic susceptibility, $\omega_{LC} = 1/\sqrt{LC}$ is the unperturbed oscillator frequency, $\omega_0 = \gamma_e B_0$, χ_0 is the static magnetic susceptibility, η is the filling factor (approximately given by (V_s/V_c), where V_s is the sample volume, and V_c is the coil sensitive volume), γ_e is the electron gyromagnetic ratio, B_1 is the microwave magnetic field, T_1 and T_2 are the relaxation times. As discussed in Ref. [13], the oscillator frequency variation due to the electron spin resonance phenomenon in the sample is, in first approximation, given by $\Delta\omega_{LC\chi} \cong (1/2)\omega_{LC}\eta\chi'$. Consequently, the oscillator frequency variation is proportional to the real part χ' of the sample complex susceptibility $\chi = \chi' - j\chi''$. The shape of the oscillator frequency variation is thus identical to that of the dispersion signal measured in conventional continuous wave experiments. However, the dependence on the microwave field B_1 is substantially different. In the conventional amplitude detection method the measured signal is linearly proportional to the precessing magnetization (i.e., to the product $\chi''B_1$ for the absorption and $\chi'B_1$ for the dispersion). In the frequency detection case, for B_1 below saturation the signal amplitude is independent of the value of B_1 and decreases as $1/B_1^2$ in saturation (in the conventional method the signal is proportional to B_1 below saturation and decreases as $1/B_1$ in saturation).

Neglecting the noise contribution of the active devices in the oscillator feedback and assuming that the frequency noise spectral density (in $\mathrm{Hz}^2/\mathrm{Hz}$) is only due to the thermal noise of the coil resistance and given by $S_v = kTR\omega_{LC}^2/(2\pi)^2V_0^2$, the spin sensitivity (in spins/$\mathrm{Hz}^{1/2}$) is given by [18]

$$N_{\min} \cong \alpha \frac{T^{3/2}\sqrt{R}}{B_0^2 B_u}\sqrt{\frac{T_1}{T_2}}, \tag{3}$$

where V_0 is the oscillation amplitude, R is the coil series resistance, B_u is the coil unitary field, T is the coil (and sample) temperature, and $\alpha \cong 20\ \mathrm{m}^{-1}\ \mathrm{kg}^{5/2}\ \mathrm{s}^{-4}\ \mathrm{K}^{-3/2}\ \mathrm{A}^{-3}$.

3. Description of the single-chip detector

Fig. 1 shows a photo and the block diagram of the realized chip, which consists of two LC-oscillators operating at about 21 GHz and 17 GHz, a mixer, and a frequency division module. The chip is manufactured in a commercially available 130 nm CMOS technology (IBM 8RF). The total chip surface, including the bonding pads, is about 1 mm^2. The total power consumption of the chip is about 20 mW at 300 K and about 6 mW at 4 K, with the oscillators bias currents set to the minimum values which enable stable oscillations. As in our previous designs [13,19], with the exception of that reported in [18], we have integrated two oscillators to perform the first down-conversion of the oscillator frequency by a mixer. The use of two oscillators and a mixer as first step in the frequency downconversion requires a frequency divider operating at 4 GHz instead of 20 GHz, which is significantly less difficult to design. The excitation/detection octagonal coils of the oscillators have an external diameter of 200 μm, a metal width of 30 μm, a metal thickness of 7.5 μm (obtained by parallel connection of the three top metal layers available in the process, two made of aluminum and one of copper), and an inductance of about 300 pH. The capacitor is realized using interdigitated aluminum fingers. The capacitance value for the two oscillators are 180 fF and 260 fF, respectively. The microwave magnetic field B_1 can be varied from 0.08 to 0.14 mT by changing the oscillator bias current I_{dc} from 1 to 5 mA. At low temperatures, a slightly lower bias current of about 0.5 mA is sufficient to guarantee stable oscillations. The lower limit is determined by the minimum transconductance of the cross-coupled pair required for stable oscillation whereas the upper limit is given by the maximum voltage swing which can be applied across the transistors in the cross-coupled pair without damaging their thin gate oxides. The value of B_1 generated by our single-chip detector is estimated by measuring the voltage at the oscillator bias node V_{Idc}. In condition of stable oscillation the oscillation amplitude $V_0 \cong V_{Idc}$ [20]. Hence, $B_1 \cong (1/2)B_u(V_{Idc}/\omega_{LC}L)$, where $B_u \cong \mu_0/d$, d is the coil diameter, and L is the coil inductance. This B_1 estimation is in agreement with saturation experiments with samples of known relaxation times.

Fig. 1 shows also the schematics and block diagrams of the mixer and frequency divider. The frequency mixer needed for down-conversion of the oscillation frequency is based on a double-balanced Gilbert cell topology (see pages 368–370 of Ref. [21]). By mixing the two oscillator output voltages a signal at about 4 GHz is obtained. The sum frequency component is filtered out by the system parasitics (i.e., a low pass filter is not necessary). The frequency divider is realized by means of current model logic (CML) D-latches with resistive load (see pages 683–699 of Ref.

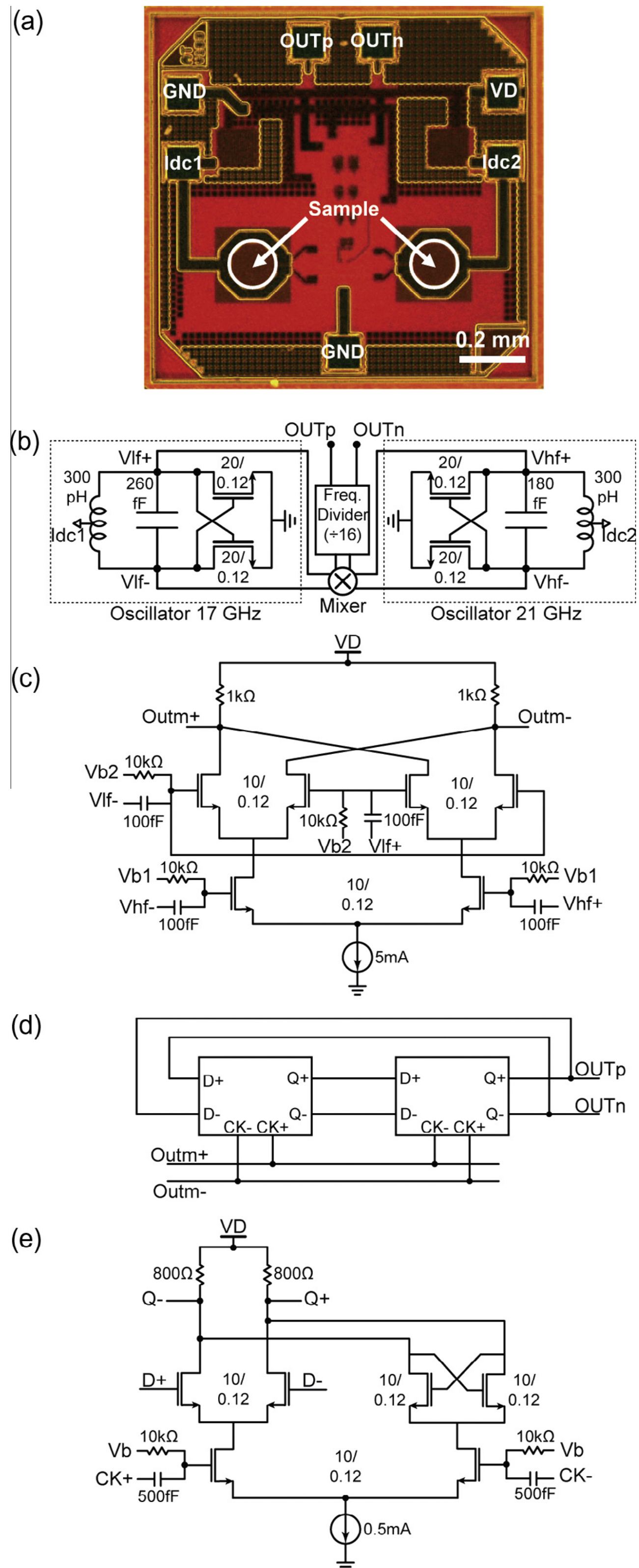

Fig. 1. (a) Microphotograph of the single-chip ESR detector. I_{dc1} and I_{dc2}: DC power supply of the two oscillators (0.5–5 mA). VD: DC power supply for the mixer and frequency-division module (1.5 V). OUTp and OUTn: differential output signal (≅220 MHz). The circle indicates the area where the samples are placed. (b) Block diagram of the single-chip ESR detector. (c) Schematics of the frequency mixer ($V_{b1} \cong 0.9$ V, $V_{b2} \cong 0.6$ V). (d) Block diagram of the frequency divider based on D-latches. (e) Schematics of the D-latch ($V_b \cong 0.6$ V).