Microelectronic Engineering 87 (2010) 2338–2342

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Ta/Si Schottky diodes fabricated by magnetron sputtering technique

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ARTICLE INFO

Article history:
Received 31 October 2009
Received in revised form 27 January 2010
Accepted 7 April 2010
Available online 24 April 2010

Keywords:
Tantalum
Schottky diodes
Barrier height
Series resistance
Sputtering

ABSTRACT

Electrical properties of Ta/*n*-Si and Ta/*p*-Si Schottky barrier diodes obtained by sputtering of tantalum (Ta) metal on semiconductors have been investigated. The characteristic parameters of these contacts like barrier height, ideality factor and series resistance have been calculated using current voltage (*I–V*) measurements. It has seen that the diodes have ideality factors more than unity and the sum of their barrier heights is 1.21 eV which is higher than the band gap of the silicon (1.12 eV). The results have been attributed the effects of inhomogeneities at the interface of the devices and native oxide layer. In addition, the barrier height values determined using capacitance–voltage (*C–V*) measurements have been compared the ones obtained from *I–V* measurements. It has seen that the interface states have strong effects on electrical properties of the diodes such as *C–V* and R_s–*V* measurements.

1. Introduction

Metal semiconductor (MS) Schottky rectifiers have a great role in power supply industry over years because of their very low forward voltage drop and switching speeds. They are also the basis of a large number of semiconductor electronic devices including microwave diodes, field-effect transistors (FETs), solar cells and photo-detectors. The characteristic parameters of Schottky diodes are affected by interface quality between metal and semiconductor [1]. It is well known that except for special fabrication, all MS devices have a thin oxide interface layer and this layer converts the MS devices to metal–insulator–semiconductor (MIS) diodes [2–4]. Therefore, the interface oxide layer at MS rectifying contacts has a crucial role in determination of Schottky diode parameters such as the barrier height, the ideality factor and the series resistance [5–8]. The understanding of the detailed mechanisms of the oxidation, reduction and etching processes involved in wafer cleaning is essential for high device yield. Moreover, after the device fabrication, its performance and stability depending on time is an important matter in the device manufacturing [1–4]. Most Schottky diodes suffer from the presence of a thin insulating layer at the metal semiconductor interface, unless it is fabricated in the vacuum, and generally, an interface layer suppose of thickness 10–30 Å [1–5].

Sputter deposition of metallic films is one of the widely used techniques for microelectronic applications [9]. Especially, it is a practical way to deposit refractory metals. Sputter deposition involves the bombardment of a target with positive gas ions and leads to the bombardment of the growing film by energetic particles [9]. It is well known that metallization procedures such as sputtering and electron beam deposition introduce defects at and close to the metal–semiconductor junction [10]. Auret et al. have found that sputter deposition introduces several electrically active defects near the surface of Ge which have also been observed after high energy electron irradiation [10]. The defects formed during sputtering process effect the performance of the devices and change the barrier height of contacts [11,12]. Depending on the application, formed defects during the sputtering process may either be beneficial or detrimental for device performance. Sawko and Bartko [13] have showed that the defects introduced during high energy electron and proton irradiation increase the switching speed of Si based devices.

In this study, Ta/Si Schottky diodes have been fabricated by dc sputtering of tantalum on *p*-Si and *n*-Si wafers. The *I–V* and *C–V* measurements of diodes have been executed to determine their electrical parameters. In addition, the effects of interfaces states caused have been observed in *C–V* and series resistance (R_s) measurements at different frequencies. It has been stated [1–4,14,15] that localized electronic states with energies inside the band gap

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doi:10.1016/j.mee.2010.04.003

exist due to the termination of the periodic structure of the crystal lattice at the surface. Simply stated, the surface states can be viewed as electronic states generated by unsaturated dangling of the surface atoms. In the laboratory environment, crystal surfaces are usually covered with layers of native oxides and organic contaminations, and surface states in the presence of these layers are modified and referred to as 'interface states'. On the semiconductor surface, the presence of the surface states in the band gap is known to 'pin' the Fermi level position of the semiconductor.

2. Experimental procedures

The Ta/Si Schottky barrier diodes were prepared using one side polished *n*-Si and *p*-Si wafers with (1 0 0) orientation and 1–10 Ω cm resistivity. Before formation of structures, both wafers were boiled 3-chloroethylene and rinsed in acetone and isopropanol by ultrasonic vibration for 5 min to remove organic contaminations. They were immersed into solution of H_2O/HF (10:1) for 30 sn in order to remove native oxide layers on the surfaces and form H terminated surfaces. Preceding each step, the wafers were rinsed in 18 MΩ deionized water. After cleaning procedures, the wafers were dried under N_2 atmosphere and inserted into the vacuum chamber. Au and Al were sputtered on the unpolished side of *n*-Si and *p*-Si substrates, respectively, to make back contacts. The thicknesses of metals were measured as 250 nm via thickness monitor of the vacuum system during sputtering processes. Both structures were annealed at 450 °C in flowing N_2 in a quartz tube furnace. After formation of ohmic back contacts, the native oxide layers formed during previous processes were removed by solution of H_2O/HF (10:1) and dried under N_2 atmosphere. Both structures were simultaneously inserted into a vacuum system. Ta/*n*-Si/Au and Ta/*p*-Si/Al Schottky rectifiers were formed by sputtering of Ta on Si substrates. The diode diameters were 1.5 mm. The *I*–*V* measurements of the diodes were performed by Keithley 2400 sourcemeter in dark and the *C*–*V* measurements of the devices were performed using Agilent HP 4294A impedance analyzer (40 Hz–110 MHz) at room temperature.

3. Results and discussion

The *I*–*V* measurements of both Ta/*n*-Si and Ta/*p*-Si executed at room temperature are shown in Fig. 1a and b. As shown in the figures, Ta/*n*-Si and Ta/*p*-Si Schottky diodes have well rectifying properties. Therefore, the simple thermionic emission theory (TET) can be used to obtain electrical properties of Ta/Si diodes. When the TET is taken into account, the current can be expressed as [14]

$$I = I_0 \exp\left(\frac{q(V - IR_s)}{nkT}\right) \tag{1}$$

where q is the electron charge, V is the applied voltage, R_s is the series resistance, n is the dimensionless ideality factor, k is the Boltzmann constant, T is the absolute temperature and I_0 is the saturation current given as;

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \tag{2}$$

with A is the diode area, A^* is the Richardson constant which is equals to 30 and 110 A cm^{-2} K^{-2} for *p*-Si and *n*-Si [15], respectively, and ϕ_b is the Schottky barrier height (SBH). The MS interfaces are an essential part of virtually all semiconductor electronic and optoelectronic devices. One of the most interesting properties of a MS interface is its SBH which is a measure of the mismatch of the energy levels for majority carriers across the MS interface. The SBH controls the electronic transport across MS interfaces and is, therefore, of vital importance to the successful operation of any semiconductor device [1–4,14,16].

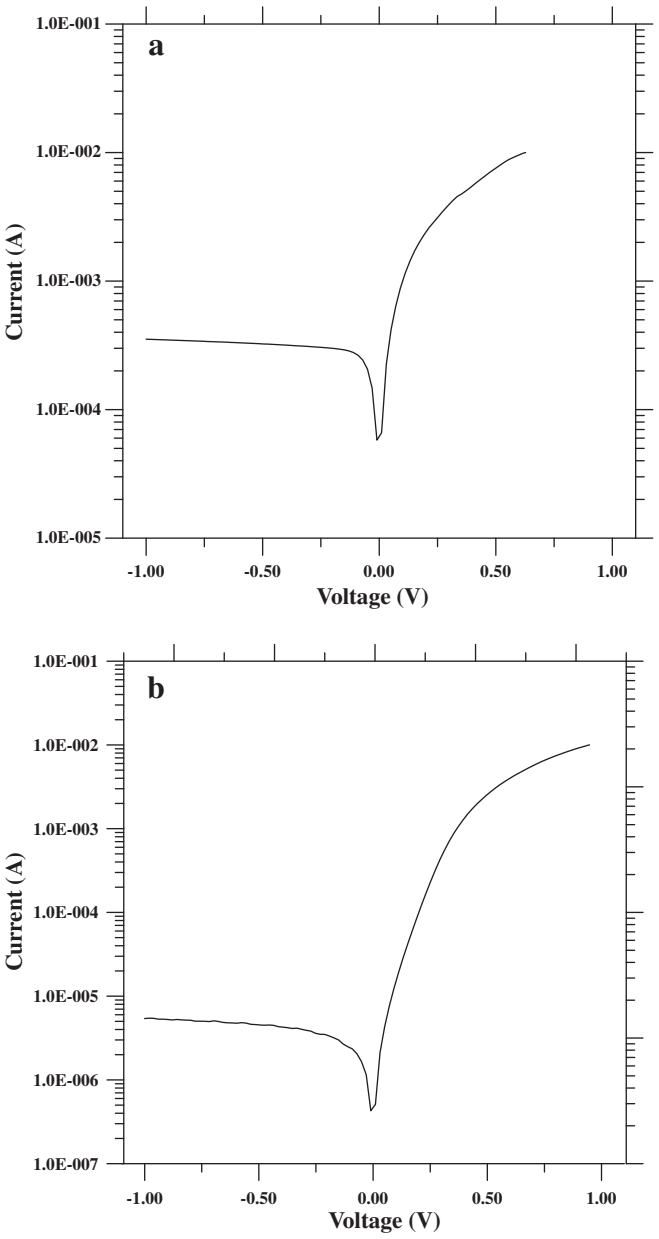

Fig. 1. Current–voltage characteristics of (a) Ta/*n*-Si and (b) Ta/*p*-Si Schottky diodes.

The ideality factor value of a device can be determined from the slope of the linear region of ln *I*–*V* curve using equation through

$$n = \frac{q}{kT}\frac{dV}{d\ln(I)} \tag{3}$$

If the ideality factor n is greater than unity, it implies the deviation from ideal diode [16,17]. That is, the ideality factor is introduced to take into account the deviation of the experimental *I*–*V* data from the ideal thermionic model and should be $n = 1$ for an ideal contact. The ideality factors of Ta/*n*-Si and Ta/*p*-Si Schottky diodes have been calculated as 1.25 and 1.15, respectively. The obtained results from *I*–*V* measurements are also shown in Table 1. The deviation from ideal diode might be due to the effects of native thin oxide layer and the interface states between the metal and the semiconductor. These values of n indicate that the device obey a metal–interface layer–semiconductor (MIS) configuration rather than ideal Schottky diode.