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Source/drain optimization of underlapped lightly doped nanoscale double-gate MOSFETs

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ABSTRACT

The impact of the spacer length at the source (L_s) and drain (L_d) on the performance of symmetrical lightly-doped double-gate (DG) MOSFET with gate length L = 20 nm is analyzed, with the type and doping concentration of the spacers kept the same as in the channel material. Using the transport parameters extracted from experimental data of a double-gate FinFET, simulations were performed for optimization of the underlapped gate-source/drain structure. The simulation results show that the subthreshold leakage current is significantly suppressed without sacrificing the on-state current for devices designed with asymmetrical source/drain extension regions, satisfying the relations $L_s = L/2$ and $L_d = L$. In independent drive configuration, the top-gate response can be altered by application of a control voltage on the bottom-gate. In devices with asymmetrical source/drain extension regions, simulations demonstrate that the threshold voltage controllability is improved when the drain extension region length is increased.
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1. Introduction

The double-gate (DG) MOSFETs are considered as possible candidates for device scaling down to the nanometer size at the end of ITRS roadmap [1], since they allow a significant reduction of the short channel effects (SCEs), such as threshold voltage roll-off, drain-induced barrier lowering (DIBL) and subthreshold slope degradation [2–6]. Moreover, in DG MOSFETs, the ultra-thin channel material is preferred to be undoped or lightly doped to eliminate adverse effects due to random microscopic fluctuations of dopant atoms.

In the subthreshold region of short-channel devices, the drain current is governed by the subthreshold leakage current that takes place when the transistor is off due to the diffusion of carriers from source to drain [7]. Therefore, as the gate length is scaled down, the off-state current (I_{off}) is increased due to the threshold voltage roll-off, which might be a severe limitation for low stand-by power (LSTP) applications. On the other hand, there is strong demand to reduce the threshold voltage in order to improve the on-state current or the high-speed operation, which in turn leads to the increase of the subthreshold leakage current or stand-by power consumption in VLSI circuits. Thus, threshold voltage controllability is an important issue for the design of circuits based on nanoscale MOSFETs. However, when the two gates of DG MOSFETs are used as independently switched gates (four terminal devices, 4T-DG MOSFETs), the devices offer the advantage of flexible threshold voltage controllability [8–11]. Recently, detailed investigation for the threshold voltage controllability was performed in terms of several device parameters in four terminal DG MOSFETs with gate length L = 78 nm [12].

In previous work, the concept of "underlapped" gate-source/drain structure was used to facilitate MOS scaling to nanoscale gate lengths [13]. The concept of underlapped channel design has been experimentally applied in bulk MOSFETs [14], polysilicon thin-film transistors [15] and vertical FinFETs [16]. Furthermore, underlapped MOSFETs have shown great potential for digital and analog applications [17–20].

It was demonstrated that I_{off} in DG MOSFETs can be reduced using a graded doping profile in the symmetric source/drain extension (SDE) regions [21]. Recently, symmetric as well as asymmetric SDE regions were used to optimize the device performance, depending on the spacer-to-doping gradient ratio [18]. The impact of symmetric spacer length on the on-state and off-state currents using two-dimensional simulations was previously analyzed by Kranti and Armstrong [22]. However, as the DG MOSFETs are scaled down, the silicon needs to be thinner for better control of the SCEs, resulting in difficulties for experimental realization of a specific doping profile in such thin layers [23].

The use of undoped or lightly-doped SDE regions with concentrations the same as the channel material seems to be an attractive

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option for future technology nodes. The absence of dopant atoms in the channel material eliminates adverse effects, such as mobility degradation and random microscopic fluctuations of dopant atoms which can lead to unwanted dispersion in the device characteristics [24,25]. In this work, the impact of SDE regions engineering is analyzed through optimization of the length of asymmetrically lightly-doped SDE regions, needed to improve the performance of 20 nm gate length *n*-channel DG MOSFETs for LSTP applications. The threshold voltage controllability by independent driving of the two symmetrical gates is also discussed.

2. Experimental and simulations

The parameters used in the simulations were extracted from the experimental transfer characteristics of *n*-channel DG FinFET device, fabricated on SOI wafers with 145 nm buried oxide thickness, following the fabrication processes described elsewhere [26,27]. Fig. 1 presents schematically the FinFET structure. The parameters of the measured device are: channel acceptor doping concentration 10^{15} cm^{-3}, donor doping concentrations of the source/drain contacts and the SDE spacers 2×10^{20} and 5×10^{19} cm^{-3}, respectively, equivalent gate oxide (EOT) thickness t_{ox} = 1.7 nm, number of fins N = 5, fin height H_{fin} = 65 nm, fin width W_{fin} = 1875 nm and gate length L = 910 nm. Since $W_{fin} \gg 2H_{fin}$ and the average electron mobility behaviour is described by the perimeter-weighted sum of the top and sidewalls mobilities [28], the mobility is mainly due to the top-gate contribution. Therefore, the FinFET can be considered as a single-gate silicon-on-insulator (SOI) MOSFET with good approximation, with the fin width W_{fin} and fin height H_{fin} corresponding to the channel width W and the silicon thickness t_{Si} of the single-gate device, respectively.

The transfer characteristics of the transistor were measured at room temperature at wafer level using a SussMicroTec LT probe station. The experimental transfer characteristics of Fig. 2, measured at drain voltage V_d = 20 mV and 1.02 V, were simulated with the Silvaco (Atlas) tools [29] using the models of drift–diffusion, band-to-band tunneling with parameters BB.A = 1.5×10^{18} V^{-2} s^{-1} cm^{-1}, BB.B = 4×10^{7} V cm^{-1}, BB.GAMMA = 2.22, Shockley–Read–Hall recombination, Shirahata's mobility model with low field mobility 500 cm^{2} V^{-1} s^{-1} and gate work-function 4.9 eV. The extracted model parameters were used for simulation of the DG MOSFETs in order to achieve short-channel devices of high performance.

3. Results and discussion

For simulations of the DG MOSFET, we have used the structure of Fig. 3 with asymmetrical SDE regions of length L_s and L_d for the source and drain extensions respectively, with L = 20 nm, W = 500 nm, t_{Si} = 10 nm and t_{ox} = 0.7 nm satisfying the specifications of ITRS 2007 [1]. The donor doping concentration for the source/drain contacts is 10^{20} cm^{-3} and for both channel and SDE regions the acceptor doping concentration is 10^{15} cm^{-3}. The doping values are chosen to be the same with those of the fabricated DG FinFETs, except the type and doping of the SDE regions which are the same as in the channel material, i.e. the SDE regions are doped with acceptors of concentration 10^{15} cm^{-3}.

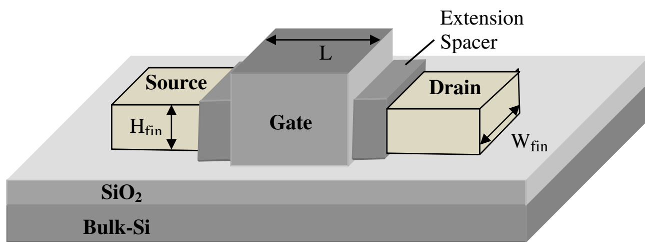

Fig. 1. Schmematic structure of the experimental FinFET.

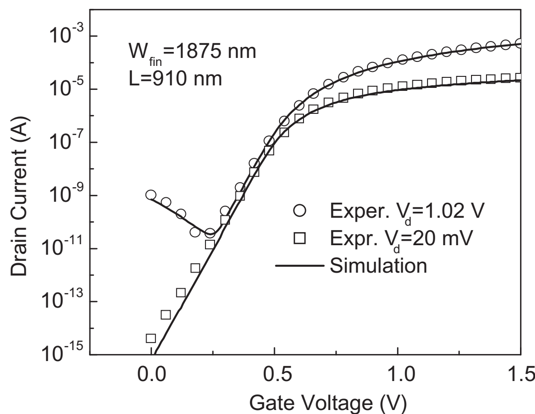

Fig. 2. Experimental transfer characteristics of FinFET with fin width W = 1875 nm and gate length L = 910 nm (symbols) at V_d = 20 mV and 1.02 V. The characteristic was reproduced with Silvaco (Atlas) simulation (solid line) using the models: drift–diffusion, band-to-band tunneling with parameters BB.A = 1.5×10^{18} V^{-2} s^{-1} cm^{-1}, BB.B = 4×10^{7} V cm^{-1}, BB.GAMMA = 2.22, Shockley–Read–Hall recombination, Shirahata's mobility model with low field mobility 500 cm^{2} V^{-1} s^{-1} and gate work-function 4.9 eV.

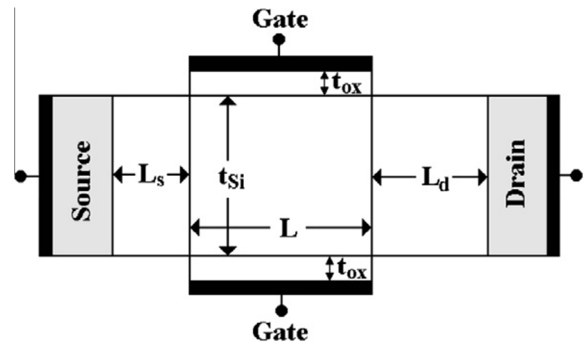

Fig. 3. Schematic diagram of the simulated DG MOSFET.

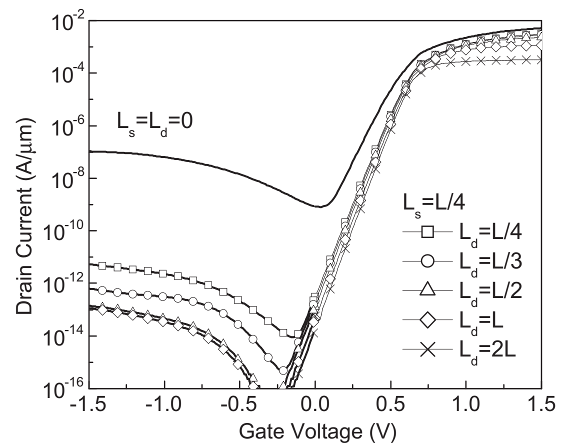

Fig. 4. Normalized transfer characteristics at drain voltage V_d = 0.7 V of DG MOSFETs with L = 20 nm, W = 500 nm, t_{Si} = 10 nm, t_{ox} = 0.7 nm, L_s = L/4 and different values of L_d, derived using the model parameters of Fig. 2.

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