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Electrical characteristics of Ge MOS device on Si substrate with thermal SiON as gate dielectric

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ABSTRACT

Metal–oxide-semiconductor (MOS) devices, using a Si substrate and a thermal SiON film as the gate dielectric on a Ge layer, have been physically and electrically characterized. The small frequency dispersion and negligible hysteresis demonstrate very few oxide traps. The efficiency of Ge surface passivation is evidenced by the acceptable interface trap density of 7.08×10^{11} cm^{-2} eV^{-1} close to midgap, which is critical for the enhancement of the carrier mobility in MOSFET devices. On the other hand, for the thermal SiON film, a higher permittivity of 4.86 can be achieved by NH_3 nitridation and a subsequent N_2O treatment of an as-grown SiO_2 film without compromising its leakage current. The conduction mechanism is confirmed to be Fowler–Nordheim (F–N) tunneling with extracted electron barrier height of 2.71 eV. Combining with these promising properties, the SiON film shows a great potential to further boost the performance of Ge MOSFETs. Most importantly, without using a Ge substrate, the SiON film on a Ge layer can be formed by the process fully compatible with incumbent ultra-large-scale integration (ULSI) technology, and hence, providing an economic way of fabricating high-performance Ge MOSFETs.

1. Introduction

Despite great advancement in high permittivity (high-κ) gate dielectrics, metal gates and strain engineering, the effort to pursue devices with higher performance never slows down. Due to the superior carrier mobility against Si, germanium (Ge) has received much attention and been regarded as a potential channel material to accommodate the ever-stringent scaling requirement for future technology nodes. One of the major challenges in achieving high-performance Ge MOS devices is to maintain a good interface property between gate dielectric and Ge channel. In spite of the water-soluble property, a thermally grown GeO_2 film has shown to possess good passivation for a Ge substrate [1]. However, extreme care should be exercised to prevent the formation of volatile GeO by the reaction between GeO_2 and Ge substrate at temperature higher than 400 °C since this reaction would leave a huge amount of interface defects and traps [2,3], and causes the degradation of the electrical properties [4]. To effectively restrict the desorption of a GeO_2 film at higher processing temperature, many research groups have explored the possibility of incorporating nitrogen or other elements into GeO_2 to form GeON [5–10], GeZrO [11], GeZrSiO [12], or GeOS [13], which were reported to have good electrical characteristics. On the other hand, many non-GeO_x based passivation methods such as surface SiH_4 [14] or PH_3 treatment [15], and AlN [15,16] or Hf_3N_4 [17] deposition have been proposed to enhance interfacial quality. Using a Si cap with SiO_2 film for Ge surface passivation is another way to realize good interfacial characteristics [18,19]. However, it requires rigorous control of the Si cap thickness to maintain desirable device performance [20]. In this work, without a Si cap, a thermal SiON film directly grown on a Ge layer was evaluated. In comparison with our previous work [21], aside from reducing the effective oxide thickness by means of thinning down the physical oxide thickness and enhancing the nitridation, this work also focuses on the analysis of interfacial property and conducting mechanism of the SiON film. Based on the negligible hysteresis, excellent frequency dispersion and interface trap density of 7.08×10^{11} $cm^{-2}eV^{-1}$ obtained from the SiON film; it shows the capability to be employed as a promising passivation method for Ge MOSFETs fabrication. Most importantly, the thermal SiON film on a Ge layer can be implemented on a Si substrate, which is not only less expensive but also compatible with existent ULSI technology.

2. Experiment

After ex-situ HF vapor treatment to maintain a native-oxide-free surface of active areas on a (1 0 0)-oriented *p*-type Si substrate, an epitaxial $Si_{0.3}Ge_{0.7}$ layer was selectively formed in the active areas by amorphous Ge deposition and a subsequent thermal annealing [22]. Thereafter, a single crystalline Ge layer can be

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formed through oxidation of the $Si_{0.3}Ge_{0.7}$ layer at 900 °C followed by a forming gas annealing at 700 °C. Then, a thermal SiO_2 film with 14.6 nm was concurrently grown on a 12-nm-thick Ge layer and served as the gate dielectric of Ge MOS capacitors. Detailed process conditions and mechanisms on implementing this film structure can be found in our previous work [21]. To further enhance permittivity of the SiO_2 film, additional thermal nitridation in NH_3 ambient and a subsequent N_2O treatment was performed at 850 °C to form a desirable nitrided oxide [23]. The physical thickness of the nitrided oxide and as-grown SiO_2 film was nearly the same after characterization by ellipsometer and TEM (Transmission Electron Microscopy). Finally, aluminum was evaporated and patterned as the gate electrode. X-ray photoelectron spectroscopy (XPS) analysis was performed to investigate bond structure of the oxide film. In order to mitigate the surface charging effect on the insulating film, a charge neutralizer (low-energy electron gun) was employed for charge compensation in the XPS measurement [24,25]. A sequence of Ar^+ ion sputtering cycles (sputtering rate of ~2.1 nm/min) interleaved with XPS measurement was utilized to obtain bond structure near the oxide surface and interface. Atomic force microscopy (AFM) was used to characterize the surface roughness of the Ge film. The eligibility for passivation was electrically evaluated by frequency dispersion, interface trap density (D_{it}) characteristics and gate leakage measurement. Note that to extract the interface trap density, Ge *n*-MOSFETs were also fabricated with the source/drain formed by phosphorous implantation and activation annealing at 600 °C for full conductance measurement [26].

3. Results and discussion

Fig. 1 manifests the cross-sectional TEM image for the sample with nitrided oxide. Besides confirming the physical thickness of 14.6 nm, smooth interface between the nitrided oxide and single crystalline Ge layer can be also observed which is beneficial for maintaining low interface traps and achieving high carrier mobility for MOS devices. Fig. 2 shows the Si 2*p* and Ge 3*d* spectra for the nitrided oxide from the XPS measurement. By comparing with the Si 2*p* spectrum of the thermal SiO_2 film which has a signal at ~103.6 eV, the strong Si 2*p* signal for the nitrided oxide at lower binding energy of 102.9 eV indicates that a large amount of nitrogen was incorporated in the oxide bulk rather than the interface to form a silicon oxynitride (SiON) film. This is similar to the results published in the literature [27]. On the other hand, the weak and broad Ge 3*d* signal at 33 eV near the oxide interface together with the nearly flat signal close to the oxide surface prove that the amount of GeO content in the nitrided oxide is negligible. In contrast to the signal near the oxide surface, the stronger signal at 33 eV near the interface can be ascribed to the fact that Ge atoms are largely repelled to the oxide interface during $Si_{0.3}Ge_{0.7}$ oxidation, and that GeO content in the oxide can be continually decreased during the reduction process through the forming gas annealing [21,28]. This result is consistent with the SIMS analysis in our previous work [21] and confirms that a thermal gate dielectric mainly composed of SiON can be directly formed on a Ge layer, which would have greater capability to improve the electrical characteristics as compared to the commonly used GeO_x-based dielectrics. Frequency dispersion of capacitance–voltage (*C*–*V*) characteristics is essential to assess the interfacial quality of a dielectric. The *C*–*V* frequency dispersion measured between 1 MHz and 1 kHz at 300 K for the capacitor with SiON film is shown in Fig. 3, and it displays less than 196 mV frequency dispersion in the depletion regime and no kinks near the inversion regime. It is worth noting that for many researches regarding the *C*–*V* characteristics of Ge MOS capacitors, inversion can be usually

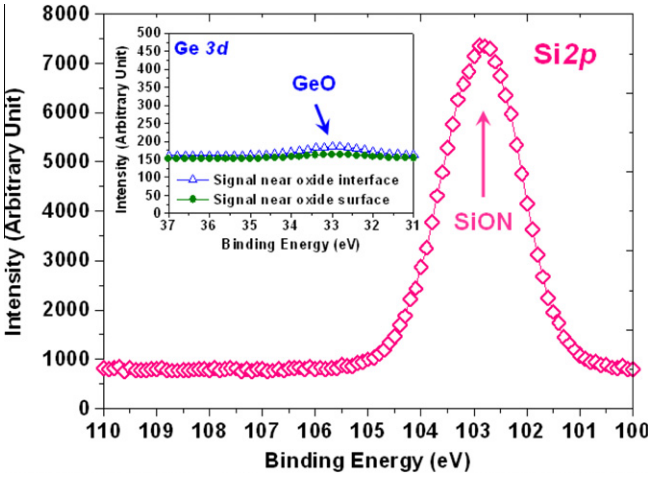

Fig. 2. XPS Si 2*p* spectrum for the nitrided oxide. The inset shows Ge 3*d* spectra for the nitrided oxide.

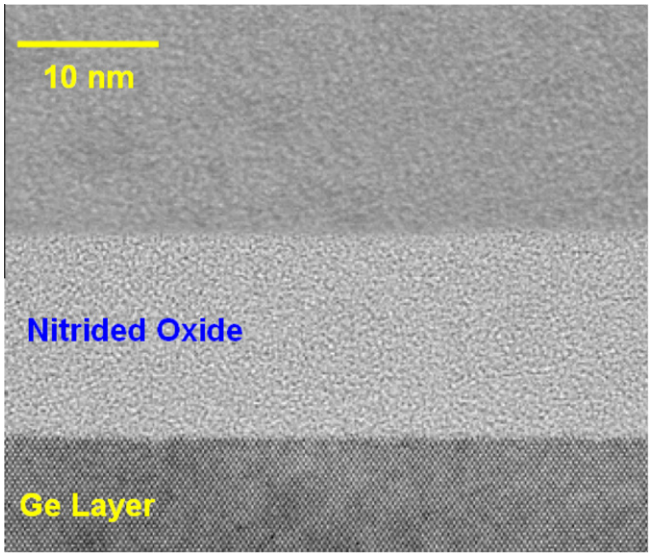

Fig. 1. Cross-sectional TEM image for the sample with nitrided oxide.

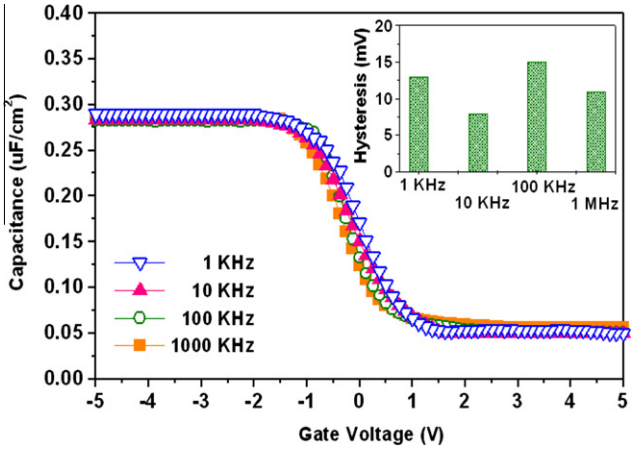

Fig. 3. Capacitance–voltage frequency dispersion characteristics for the capacitor with SiON film. The inset is the comparison of hysteresis measured by ±5 V sweep at different frequencies for the capacitor with SiON film.