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Integration of high-performance RF passive modules (MIM capacitors and inductors) in advanced BEOL

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ABSTRACT

Passive components are key elements for the integration of system-on-chips, fixing circuit performance and down-scaling capability. The integration of MIM capacitors and inductors among Cu BEOL of CMOS technologies faces many challenges and requires technological innovations in the field of material, process, and architecture developments. An overview of the main challenges and investigated solutions is presented in this paper.

1. Introduction

The tremendous expansion of telecommunication and multimedia applications pushes for the integration of complete system-on-chip (SOC) merging analog and digital processing units. Such mixed-signal integrated circuits embed CMOS and bipolar transistors as well as key passive components, i.e. inductors and capacitors, required in many applications as amplifiers, mixers, voltage-controlled oscillators, filters, resonators. These passive elements hardly shrink from one technology node to the other and thus occupy an increasing silicon footprint, compromising circuit scalability and cost. This point is illustrated in Fig. 1, which presents the impressive area covered by inductors and MIM capacitors in the layout of a typical RF receiving circuit embedded in mobile phones using the 90 nm technology node. Increasing the density of passive components is mandatory. Moreover, passive components performance is limited due to the proximity of lossy Si substrate (typical resistivity range 5–50 Ω cm) and surrounding metallization.

So, the integration of these elements in the back-end of line (BEOL) networks of chips faces many challenges. They are mainly related to the need for a progressive scaling down of passive dimensions following the Moore's law while achieving the adequate level of electrical performance, especially in the radio frequencies (RF) range [1]. The reliability performance and compatibility with Cu interconnects also have to be assured. Indeed, several technological innovations are needed to meet specifications.

An overview of the main development trends and technological solutions under investigation in the literature is reported in this paper. In Section 2, the figures of merits, challenges and technological innovations associated to the realization of inductors on Si substrate are presented. In Section 3, the evolution of MIM capacitors integration is developed in terms of material innovation and new architecture developments.

2. Integration of inductors

2.1. Figures of merit

Inductors are widely integrated among amplifying, filtering, matching, and oscillating applications. They are designed as planar spirals to reach a high inductance value by taking advantage of mutual inductance effects, and integrated in the less resistive upper interconnect levels to minimize both metal losses and capacitive couplings. A ground reference connected to the substrate is added to isolate the inductor from neighboring components, and to collect the parasitic currents generated among Si by capacitive and inductive couplings.

A simplified lumped model for a typical inductor is proposed in Fig. 2. L_S stands for the inductance value, R_S is the metal losses of the spiral, and C_P represents the parallel capacitance. C_{OX} models the electrical coupling with the ground reference, and R_{GND} is the resistance seen by the return currents. Finally, the inductance L_E, the mutual inductance M and the resistance R_E correspond to the magnetic losses induced by Eddy currents generated by the magnetic field penetration into the Si substrate.

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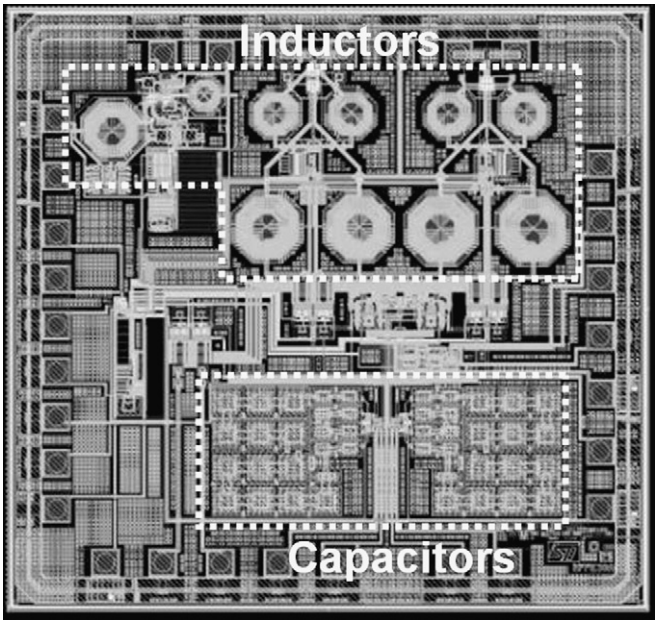

Fig. 1. Layout of a RF reception circuit for mobile phones integrating inductors and MIM capacitors.

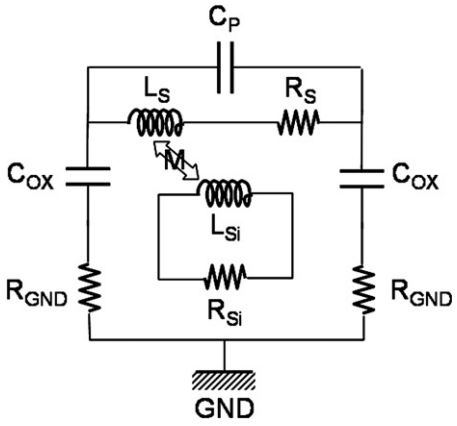

Fig. 2. Equivalent electrical model of an integrated inductor.

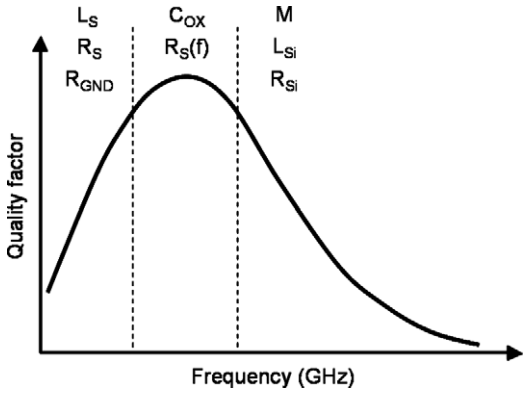

Fig. 3. Typical evolution of Q-factor and critical parameters distribution versus frequency.

Performance requirements are a high inductance density, to minimize Si footprint, a high quality factor (Q-factor), which stands as the ratio between the stored magnetic energy and losses, and a high resonance frequency. Typical values for CMOS technologies are inductance of 1–5 nH covering between 10,000 and 250,000 μm^2 with a Q-factor around 10 [2]. This Q-factor suffers from the resistive return path for currents, parasitic capacitances, metal losses, skin effect, Eddy current generation in inductor coil and neighboring metallization, and both electric and magnetic couplings with the lossy Si substrate (Fig. 3) [3].

2.2. Reduction of metal losses

In the low frequency range, *Q*-factor increases proportionally with frequency, being mainly fixed by L_S and the resistive elements R_S and R_{GND}. The purpose of the ground reference is to collect the displacement currents generated by parasitic couplings between the inductor and the substrate. Reducing R_{GND} from 300 Ω for a standard Si to a value between 1 and 3 Ω for a Cu ground plane added in the first metal level M1 improves the *Q*-factor and prevents electrical coupling with substrate. This ground shield is patterned to avoid the generation of Eddy currents because of the magnetic fields created by the inductor. Different shielding geometries have been reported, leading to *Q*-factor improvement by up to 50% [4].

Different methods have been investigated in order to reduce R_S. The simplest approach consists in stacking multiple metal levels connected in parallel to achieve low R_S values, taking benefit from the integration of additional interconnect levels at each generation. The drawback of this technique is the increase of the capacitance C_{OX} as the distance between the inductor and the ground reference decreases, thus reducing the self resonant frequency and the *Q*-factor at high frequencies, limiting the *Q*-factor improvement to 20% [5]. The most interesting alternative is the integration of a copper metal level thicker than usual interconnects layers, providing a low loss metallization for inductor coils. Exceptional *Q*-factor improvements by a factor up to 100% have already been demonstrated [6,7].

However, this serial resistance exhibits a strong frequency dependent behavior because of the skin effect, inherent to all conductors, and the self-induced Eddy currents, which increasingly impacts R_S as frequency grows. The magnetic field generated by the inductor induces circular Eddy currents within the coil, causing non-uniform current flow and degrading the *Q*-factor. Eddy currents are particularly intense among the inner turns [8]. Different solutions have been reported: (i) removing the inner turns limits the impact of Eddy currents but also reduces the inductance value [9], or (ii) optimizing the width of the coil along the spiral using complex models of serial resistance frequency dependence [10].

A simple solution is proposed: the division of inductor coil into multiple parallel narrow strips less exposed to magnetic induction of Eddy currents. Electromagnetic simulations were performed to extract current distributions for a single 16 μm wide coil (Fig. 4a) and four 3.7 μm wide strips separated by 0.4 μm to reach the same total width (Fig. 4b). As a result, R_S static value is increased due to the reduction of the conducting section, but, as Eddy currents are lowered in each narrow strip, R_S increase with frequency is slowed down leading to a *Q*-factor improvement of 20% (Fig. 5). For frequencies above 1.2 GHz, stranded strips lead to better performance. This approach also presents the advantage of reducing the dishing effect occurring during the chemical and mechanical polishing (CMP) step by reducing the metal local density, enabling to widen the coil above maximum DRM and further reduce R_S.

Another concern with Eddy currents is the losses induced within surrounding metallization, especially the copper dummy tiles that are introduced to homogenize copper density. In most of the