Microelectronic Engineering 85 (2008) 2032–2036

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

# Characterization of Ni/Ho and Ni/Er fully silicided metal gates on $SiO_2$ gate dielectric

Bao-Min Wang, Guo-Ping Ru *, Yu-Long Jiang, Xin-Ping Qu, Bing-Zong Li, Ran Liu

*State Key Laboratory of ASIC and System, Department of Microelectronics, Fudan University, Shanghai 200433, China*

ARTICLE INFO

*Article history:*
Received 26 March 2008
Received in revised form 18 April 2008
Accepted 18 April 2008
Available online 30 April 2008

*PACS:*
73.30.+y
73.40.Qv
85.40.Ls

*Keywords:*
Fully silicided (FUSI)
Metal gate
Work function (WF)
Flatband voltage ($V_{FB}$)
Interface trap

ABSTRACT

This paper investigates the effects of Ho and Er on the sheet resistance and crystallinity of Ni(Ho) and Ni(Er) silicides, the work function (WF) modulation of Ni(Ho) and Ni(Er) fully silicided (FUSI) gate electrodes on $SiO_2$ dielectric, and the FUSI gated $SiO_2$/Si interface trap properties by using high-frequency capacitance–voltage (*C–V*) and photonic high-frequency *C–V* measurements. It was found that as the thickness percentage of rare earth (RE) metal in the Ni(Ho) or Ni(Er) increases, the sheet resistance of the silicide increases. The crystallinity decreases in the Ni(Ho) and Ni(Er) silicides, and the crystallinity decreases as the Ho thickness percentage increases. As the thickness percentage of Ho in the Ni(Ho) increases from 13% to 30%, the flatband voltage ($V_{FB}$) shift increases from −0.19 to −0.27 V. The $V_{FB}$ shifts negatively 0.17 V due to 10% Er incorporation in the Ni(Er). The $V_{FB}$ shift can be attributed to the effective WF decrease which may be due to the crystallinity decrease of Ni(Ho) and Ni(Er) FUSI. The interface trap density $D_{it}$ calculated from the photonic high-frequency *C–V* curves is in good agreement with that calculated from the high-frequency and photonic high-frequency *C–V* curves. The Ho or Er addition does not increase the $D_{it}$.



## 1. Introduction

Metal gate electrodes are required for 45-nm node complementary metal–oxide–semiconductor (CMOS) devices to replace poly-Si in order to achieve equivalent oxide thickness (EOT) < 0.65 nm according to ITRS [1]. Metal gates have many advantages over poly-Si gates, such as no poly depletion effects, no boron penetration, very low resistance, and suppressed remote charge scattering [2]. Recently Intel and IBM have committed to putting Hf based high-*k* gate dielectrics and metal gate electrodes into production for the 45 nm generation. Three major metal gate integration schemes have been reported: fully silicided (FUSI) gate, metal inserted poly-Si stacks gate, and replacement gate [3].

Ni-based FUSI metal gate for dual-gate CMOS applications has been investigated extensively due to its excellent compatibility with the conventional CMOS field effect transistor fabrication process [4–12]. The NiSi electrode has a midgap work function (WF) [4], but threshold voltage ($V_{th}$) design requires band-edge WFs of gate electrodes for bulk and partially depleted silicon-on-insulator transistors (close to conduction band for NMOS, and close to valence band for PMOS) [6]. Several methods to tune WF were demonstrated such as phase control (NiSi for NMOS, Ni-rich silicide for PMOS), dopant implantation (B, P, As, Sb, Al), and alloying, which allow to reach appropriate WF and $V_{th}$ values [4–10,12]. However, the dopant implantation induced $V_{th}$ shift for Ni FUSI electrodes on Hf-based high-k gate dielectrics, such as HfSiON, is much smaller than that for Ni FUSI on a $SiO_2$ gate dielectric [2,4]. And the dopant dose should be carefully optimized because some EOT loss and adhesion problems may occur at high ion implant doses. Especially, NiSi film doped with Sb and As is easy to peel off [2,6,10]. Another method to adjust $V_{th}$ is to alloy nickel silicides with proper elements that help to move the WF toward band edges. And the reason was believed to be possibly due to the segregation of the alloying element at the FUSI/dielectric interface [2]. Rare earth (RE) metals such as Yb, Tb, Gd, Ho, and Er, have low WFs ranging from 2.5 to 3.4 eV [13]. And recently Yb-, Tb-, and Gd-alloyed Ni-silicide gates have been used to demonstrate low WF values [5,8–9]. In this work, we investigate Ho and Er-alloyed Ni-silicide FUSI gate process, the effect of Ho and Er on the sheet resistance and crystallinity of Ni(Ho) and Ni(Er) FUSI, and the WF modulation effect of Ni(Ho) and Ni(Er) FUSI gate electrodes on $SiO_2$ dielectric.

## 2. Experimental

The starting material was a p-type Si (100) substrate with a resistivity of 6–10 Ω cm. After standard RCA cleaning and the treatment with diluted HF, thermal oxide with thickness of 5 and

* Corresponding author. Tel.: +86 21 6564 3561; fax: +86 21 6564 3768.
*E-mail address:* gpru@fudan.edu.cn (G.-P. Ru).

0167-9317/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2008.04.025

10 nm was grown by dry oxidation, and 110 nm undoped poly-Si film was deposited by low-pressure chemical vapor deposition onto the grown oxide film. For full silicidation, five multilayer structures of Ni(76 nm)/Ho(11 nm), Ni(66 nm)/Ho(11 nm)/Ni(10 nm) (denoted as Ni(13%Ho)), Ni(51 nm)/Ho(26 nm)/Ni(10 nm) (denoted as Ni(30%Ho)), Ni(76 nm)/Er(8.5 nm) (denoted as Ni(10%Er)), and Ni(61 nm)/Er(28.5 nm) (denoted as Ni(32%Er)) were deposited on poly-Si with 10 nm $SiO_2$ by ion beam sputtering. Silicidation process was performed using rapid thermal annealing (RTA) at 600 °C for 60 s, except for Ni(32%Er) with RTA at 700 °C for 60 s. Prior to metal deposition, native oxide was etched away by diluted HF. Ni FUSI gates were also fabricated by using a Ni thickness of 76 nm to fully react with 110 nm poly-Si on 5 and 10 nm $SiO_2$. The silicidation was carried out by RTA at 510 °C for 90 s. 66 nm Ni was also prepared as a reference for incomplete silicidation by RTA at 530 °C for 120 s on 5 nm $SiO_2$. Un-reacted metals were removed by sulfuric peroxide mixture (SPM) ($H_2SO_4$:$H_2O_2$ = 4:1). Metal gate stacks were then patterned by wet etch to form capacitors with an area of $1.77 \times 10^{-4}$ $cm^2$. All the Ni(RE) multilayer structures were also deposited on n-Si substrate, and silicidation process was performed using RTA at different temperatures for 60 s. Un-reacted metals were removed by SPM.

Four-point probe was used for sheet resistance $R_s$ measurements. X-ray diffraction (XRD) and Raman spectroscopy were used for analyzing the silicide phase and crystallinity. High-frequency capacitance–voltage ($C$–$V$) measurements were done by Agilent 4294A precision impedance analyzer at 1 MHz in dark while photonic high-frequency $C$–$V$ measurements were done at 1 kHz under LED illumination. Flatband voltage ($V_{FB}$) and EOT were extracted from high-frequency $C$–$V$ curves, and quantum effects were considered for the EOT extraction by using NCSU $C$–$V$ program [14]. Interface trap density $D_{it}$ was calculated from photonic high-frequency $C$–$V$ curves, and also from the comparison of high-frequency and photonic high-frequency $C$–$V$ curves.

## 3. Results and discussion

Fig. 1a and b shows transformation curves for Ni(76 nm)/Ho(11 nm), Ni(13%Ho), Ni(30%Ho), Ni(10%Er), and Ni(32%Er) silicides after selective etch (SE) on n-Si, and sheet resistance of silicides after SE on undoped poly-Si, respectively. To understand the stages of the Ni(Ho) and Ni(Er) reaction with n-Si and poly-Si, the sheet resistance measurements were conducted on each wafer. It can be seen from Fig. 1a that Ho and Er slow down the formation of low-resistive NiSi, as Ho or Er thickness percentage increases. Especially, little low-resistance Ni-silicide is formed on Ni(76 nm)/Ho(11 nm) samples until 700 °C, and Ni(32%Er) has very high sheet resistance until 900 °C, indicating little NiSi formation on n-Si. While Ni is a moving species during Ni-silicide formation, silicon is expected to updiffuse and react with Ho or Er to form $RESi_2$ at relatively high temperature. The presence of RE thus slows down the silicidation process. Fig. 1b shows that sheet resistance of Ni, Ni(13%Ho), Ni(30%Ho), Ni(10%Er) and Ni(32%Er) silicide formed on undoped poly-Si is 1.4, 1.8, 3.1, 2.1, and 4.9 Ω/sq, respectively. The sheet resistance increases as the Ho or Er thickness percentage increases. Such a trend should not be a surprise because firstly, Er interlayer in the Ni(61 nm)/Er(28.5 nm) bilayer structure retards the NiSi formation, secondly, the resistivities of Ho silicides are larger than 100 μΩ cm, which are appreciably higher than that of NiSi [15], and thirdly the crystallinity decrease of Ni(Ho) and Ni(Er) silicide (as discussed below) may increase the resistivity.

Fig. 2 shows XRD spectra of the silicides after SE formed from Ni on undoped poly-Si, Ni(13%Ho) on n-Si, Ni(30%Ho) on n-Si, and Ni(10%Er) on undoped poly-Si. In Fig. 2, we can see a strong peak at $2\theta \approx 33.0^{\circ}$ in some samples. The corresponding interplanar spacing coincides with (200) diffraction of Si. The Si (200) diffraction is forbidden due to its vanishing structure factor, however multiple diffraction may occur from the planes of a single crystal resulting in a final diffracted beam, which may appear to correspond to a forbidden diffraction [16]. The dominant phase is NiSi, with secondary

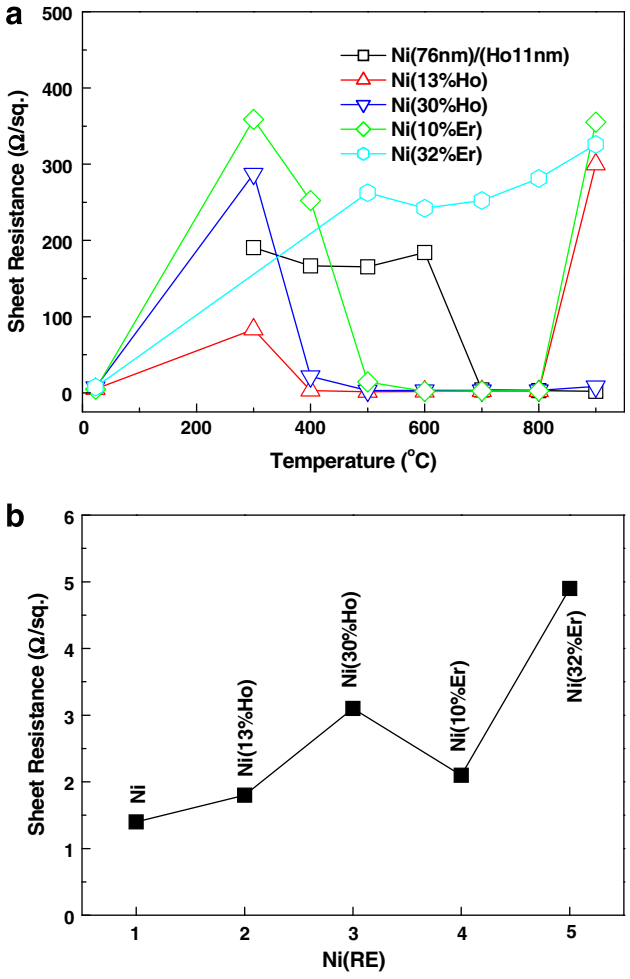


**Fig. 1.** (a) Transformation curves for Ni(76 nm)/Ho(11 nm), Ni(13%Ho), Ni(30%Ho), Ni(10%Er), and Ni(32%Er) silicides after SE on n-Si, and (b) sheet resistance of the silicides after SE on undoped poly-Si.

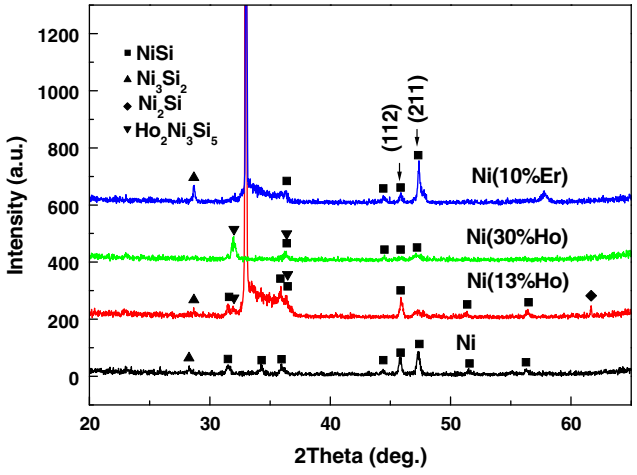


**Fig. 2.** XRD spectra of the silicides after SE formed from Ni on undoped poly-Si, Ni(13%Ho) on n-Si, Ni(30%Ho) on n-Si, and Ni(10%Er) on undoped poly-Si.