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Extensive investigations of temperature influence on barrier integrity during reliability testing

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ABSTRACT

Investigation of stress migration phenomena is one of the key aspects to characterize metallization reliability. Typical test methodologies are investigations of resistance shifts at wafer-level or package-level temperature storage tests under a temperature range between 150 °C and 275 °C. During these tests a very limited resistance increase dependent on the test structure is allowed. Most recently we encounter unusual resistance shift at the highest stress temperature which did not yield classical stress voiding detectable by failure analysis. We found changes in barrier integrity explaining the resistance shift by barrier oxidization. This has been verified by specially prepared material as well as extensive failure analysis investigation.

1. Introduction

Usual lifetimes of semiconductor products are several years. For a given technology a reliability assessment must be reached within weeks or less. This is only possible with highly accelerated lifetime tests. One of the key acceleration parameter is temperature. Back-end of line tests such as electromigration and stress migration use testing temperatures in the range of 150–350 °C [1]. This thermal load of several hours to days could have a significant impact on the structure and composition of the tested samples. Highly accelerated reliability testing show changes in performance due to temperature annealing during test compared to standard tested reliability tests [2,3]. Additionally, annealing investigations without the focus of reliability testing and therefore performed at much higher temperatures as of the reliability tests indicate changes in barrier integrity [4–6].

Balancing the highest acceleration with the lowest possible change in physics, structure or composition is essential to ensure realistic lifetime extrapolations for a given test. Therefore these results will have an important impact on testing strategies when setting new upper limits for testing temperature, e.g. temperature-time product limits.

Stress migration phenomena are fairly well understood. Common sense is that different stress states relax along stress gradient due to build in TCE mismatch. Therefore in most cases it is possible to understand the root cause of different stresses and counter react by design/geometry or material changes. Mostly stress migration behavior is characterized by design (DRC) and non-design rule compliant (non-DRC) structures and void characterization by failure analysis. The DRC structure need to stay within the given maximum resistance increase limit, The non-DRC structures are allowed to fail the resistance criterion but give good indication of geometrical dependence of the investigated process.

In this paper we show extensive physical failure analysis results with the focus on stress migration tested material showing unusual behavior with respect to temperature and resistance. Starting point of this investigation was to understand resistance shifts in stress migration tests on DRC structures at 275 °C (Fig. 1) which did not yield the "typical" stress migration voiding after 1000 h testing [7] (Figs. 3 and 4).

To understand this phenomenon we investigated specially prepared material with respect to changes in barrier integrity. We found evidence that the barrier turns into a Ta_xO_y layer which is known to have higher resistance than Ta based barrier only.

2. Experimental setup and results

For this investigation we used two different sets of material. The first set consists out of fully build back-end of line stack, patterned wafers. This material enables to closely investigate the resistance behavior and gives the possibility to catalogue the different

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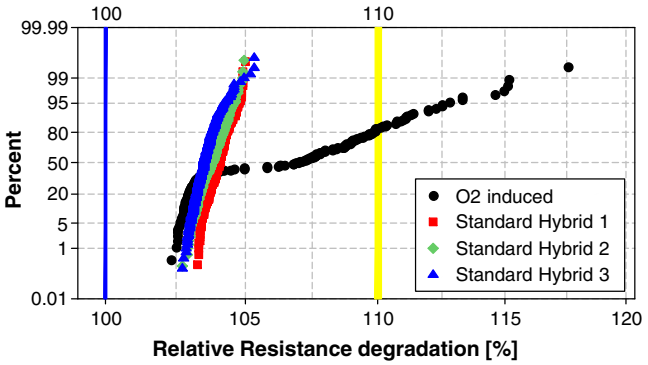

Fig. 1. Relative resistance change comparison between standard and O2-induced PVD-Cu seed samples.

material groups. The material was produced in 90 nm node technology with nine metal layers. The samples have been passivated by nitride and polyimide. This set consists of three sub-sets (Fig. 12).

(1) Dielectric is SiCOH only.
(2) Dielectric is hybrid-SiCOH with standard barrier-seed process. Here on trench level the dielectric is SiCOH, whereas the dielectric in the via-level is SiO_2 based.
(3) Dielectric is hybrid-SiCOH where we introduced oxygen during PVD-Ta/Cu deposition to simulate a high oxygen concentration directly in the system.

Secondly, blanket wafers with a stack reproducing the via bottom area were built. Here, we deposited galvanic-Cu right on top the Si substrate. On this "lower-interconnect" the barrier-seed process with 6 nm PVD-Ta, followed by PVD-Cu seed was used and "passivated" with a SiCN layer (Fig. 13). The main focus of this investigation was to ensure good access for failure analysis in particular for SIMS and EELS investigation to the "via bottom".

On the first material set we performed stress migration tests on wafer-levels at 175 °C, 225 °C and 275 °C for 1000 h. The resistance was measured (either on two pad or Kelvin structures) every 250 h by removing the wafers from the oven and testing the material on commonly used fully-automated wafer-level test systems. As test structures we used two layers via chains where the 10 μm long links are connected by single vias on each end to the link in the other layer. These chains exist in all layers and give the possibility to characterize the whole layer stack. The link width varied from around 100 nm (DRC structures) to several micrometer width (non-DRC). We used 10% and 20% resistance increase as a failure criterion.

Whereas we did not see any obvious difference in 175 °C and 225 °C testing, the 275 °C results show different behavior for the three different sub-sets. Surprisingly the full-SiCOH (set 1) samples show resistance increases of more than 20% though they have exactly identical designed test structures. Additionally the hybrid-SiCOH set with additional oxygen (set 3) (introduced during barrier-seed deposition) show exactly the same behavior as the full-SiCOH samples (set 1) whereas the hybrid-SiCOH without additional oxygen was absolutely clean (set 2). This effect could be already observed after the first read out (250 h). Since the main contribution to the resistance was assumed to be the via bottom barrier (Ta has a much higher resistivity than Cu) we built and used the blanket wafer material to do closer investigation of this area. To provide the same boundary conditions the blanket wafers have been stored in ovens at 275 °C (250 h and 500 h) and 300 °C (250 h) which exactly copies the conditions of the first read out of the standard stress migration testing on the patterned material. Also a non-stored wafer was characterized for comparison.

3. Physical failure analysis

Extensive TEM investigation has been done on the blanket material (Fig. 6). This material was built to reproduce the environment in the via bottom area for easy access to failure analysis techniques. The different sets of material have been investigated. Looking at the wafer which did not see high temperature storage (HTS) the characterization reveals that the top-interface between the Ta-barrier and the PVD-Cu was very flat and even. The lower interface between the barrier and the copper was somehow rough. Additionally no amorphous areas above or below the Ta-barrier could be found. Only very thin intermixing layers could be observed (Fig. 6a). The stored samples reveal clearly visible amorphous areas below the Ta-barrier (Fig. 6b–d). These amorphous areas form an inhomogeneous layer under the Ta-barrier which is more or less of the same thickness for all storage times. Using combined EELS/EDX analysis the amorphous areas have been proven to be Ta oxide (Fig. 7).

SIMS investigations on these samples clearly show differences in oxygen profile. Fig. 8 shows the Cu signal with a dip in the Ta-barrier area. The tail of the TaO_2 signal in this plot is very likely related to smearing during sputtering the rough lower interface from Ta to galvanic-Cu. A high resolution investigation of the oxygen signal clearly shows a shift of oxygen during stressing. The unstressed sample shows a Ta-peak which is closer to the Ta-PVD-Cu interface than the samples with temperature history (Fig. 9).

4. Discussion

Summarizing these two investigations the oxidation of the Ta-barrier at the Ta-galvanic Cu interface is most likely to occur. To verify the proposal of Ta-barrier oxidation, we produce full-stack samples with a small amount of oxygen introduction during PVD-Cu deposition (on the hybrid stack system). This was done

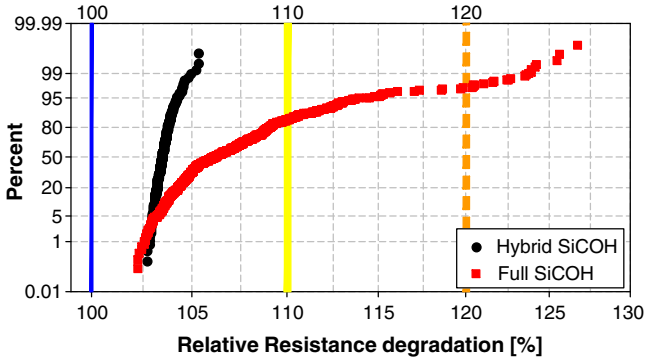

Fig. 2. Relative resistance change comparison between hybrid and full-SiCOH stack.

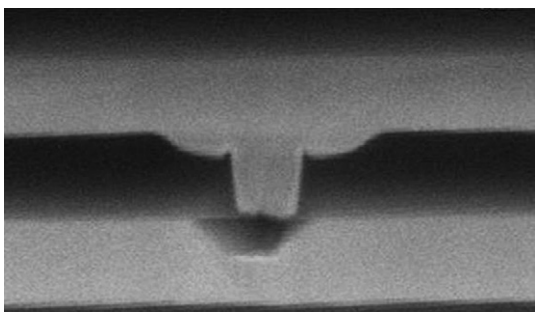

Fig. 3. "Classical" stress migration void after testing.