

Evaluation of Air Gap structures produced by wet etch of sacrificial dielectrics: Critical processes and reliability of Air Gap formation

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Abstract

Two Air Gap technologies were investigated concerning critical process steps. Both approaches use SiO₂ for sacrificial material and buffered HF wet etch chemistry. These critical processes include pre-wet-etch-concerns and wet-etch-concerns. The results of a special spacer etch-back process are shown. A buffer layer of SiO₂ was introduced to relax the requirements on the dry back-etch process. The oxidation of SiC and SiCN films during dry etching and resist stripping is an issue of both technologies, because this may lead to an undercut of the interconnect lines during the buffered HF treatment. Nevertheless, this can be successfully avoided by the application of appropriate oxygen (O₂) free process media. Furthermore, the shifting of mechanical behaviour of such structures as a result of wet-etch treatment is investigated. The intrinsic stress of cantilever SiC films has the capability to cause pull-off forces to interfaces which may result in film delamination.

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1. Introduction

The formation of Air Gap structures is a promising alternative to achieve low-*k* or even ULK performance for future technology nodes. It has been shown that k_{eff} values of 2.5 or even significantly lower are well achievable for different integration schemes and MPU generations [1–3]. Beyond this, several Air Gap approaches largely share conventional processing of Cu and SiO₂. One of the main issues of low-*k* integration is the degradation of the thermal behaviour of the interconnect system. This is due to their

low thermal conductivity. In contrast to this hybrid Air Gap integration schemes achieve a comparable thermal behaviour to interconnect systems which utilize exclusively SiO₂ for IMD [4]. A general classification of published Air Gap approaches was given by Gosset et al. [5]. This comprises void formation via non-conformal CVD deposition and the application of sacrificial layers between the copper lines. Two similar sacrificial layer Air Gap approaches (“mask” and “spacer”) were developed at TU Chemnitz. The feasibility of both variants was shown [6] and they were characterized in terms of their electrical properties (reduction of inter-metal capacitances and k_{eff}) [1]. The removal of the sacrificial material (PECVD SiO₂) is performed by buffered HF solution (Air Gap formation). This paper is related to critical processes during the fabrication and formation of such structures. These can be assigned to three categories: pre-wet-etch-concerns, wet-etch-concerns, and processing of Air Gap closure.

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2. Experimental

The general technological sequences of both principles are shown in Figs. 1 (“mask” approach) and 2 (“spacer” approach). The metal lines and dielectric barriers align the wet etch treatment. The functional films for etch stop and masking of both Air Gap approaches consist of PECVD SiC:H.

2.1. Pre-wet etch processing

This includes the process steps up to the states of Figs. 1a and 2a. A conventional Copper-Single-Damascene technology with only slight changes for the “spacer” approach is used. This comprises a conformal deposition of a PECVD SiO₂ spacer and an anisotropic etch-back of this layer immediately before the metal deposition. A schematic

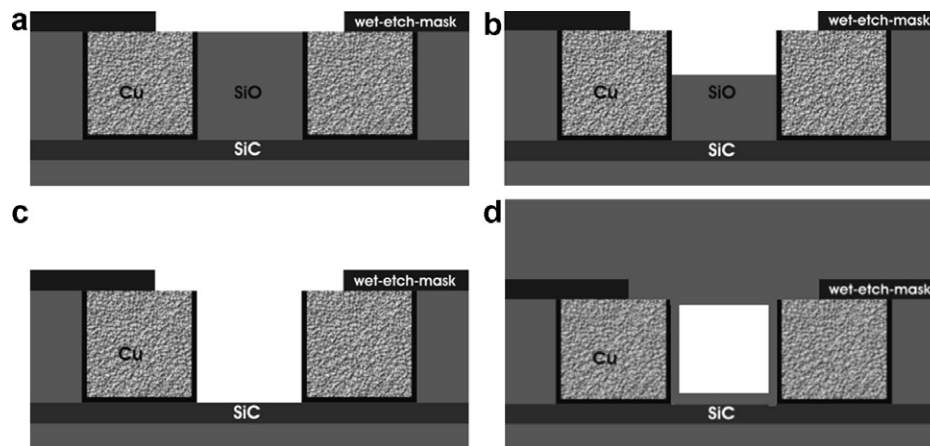


Fig. 1. “Mask” approach: (a) after CMP and “wet-etch-mask” patterning; (b) partially wet etched; (c) fully removed USG dielectrics; and (d) sealed Air Gap structures (using non-conformal CVD).

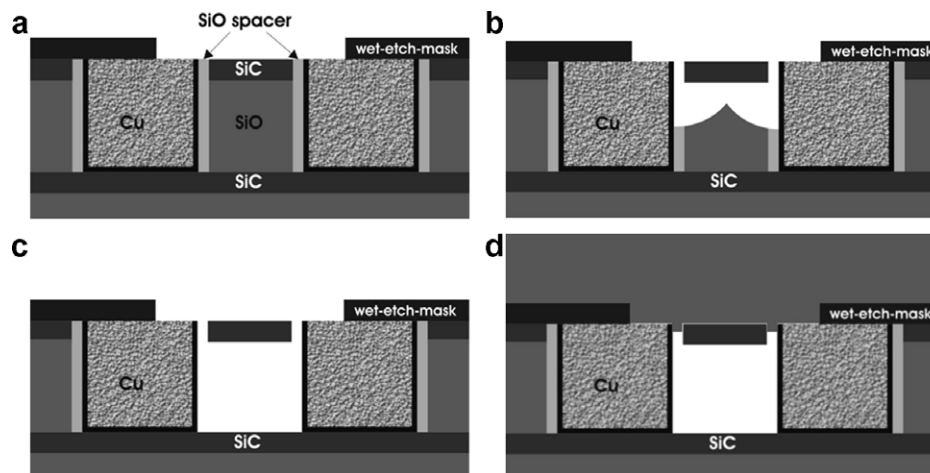


Fig. 2. “Spacer” approach: (a) after CMP and “wet-etch-mask” patterning; (b) spacer opening and partially wet etched; (c) fully removed USG dielectrics; and (d) sealed Air Gap structures.

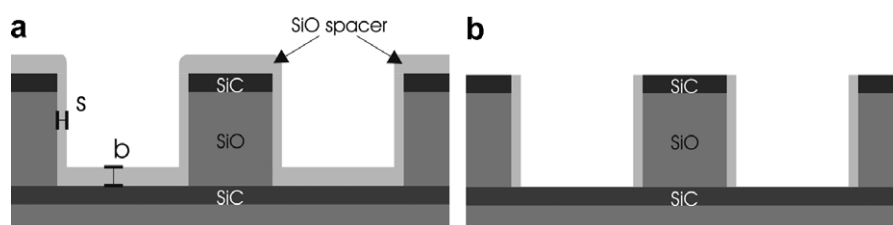


Fig. 3. (a) Conformal deposition of spacer material. (b) Anisotropic etch-back processing.

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