Available online at www.sciencedirect.com
ScienceDirect
Microelectronic Engineering 84 (2007) 2729–2732
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

Analysis of low temperature RTP needs for IC metallization

Igor J. Malik *, Michel Ouaknine, Takashi Fukada, Woo Sik Yoo

WaferMasters, Inc., 246 East Gish Road, San Jose, CA 95112, USA

Received 11 May 2007; accepted 21 May 2007
Available online 7 June 2007

Abstract

We discuss the desirable properties of an RTP tool and process for low temperature (<700 °C) applications. We contrast two different approaches for heating the substrates – a "cold-wall" system in which the energy is delivered as photons, and a "hot-wall" system where heat convection and conduction are the dominant heat transfer mechanism. We present arguments for why "hot-wall" systems have distinct advantages for most processes in the low temperature regime and demonstrate our conclusions on examples of Ni and Co silicidation process.

Keywords: Rapid thermal processing (RTP); Isothermal cavity; Nickel silicide; Cobalt silicide; Repeatability

1. Introduction

Rapid thermal processing (RTP) has gained wide-spread acceptance in implant anneals in the 1990s [1]. The majority of the RTP systems used for implant anneals, that are typically performed above 1000 °C, are lamp-based (a "cold wall" approach), i.e., the energy is delivered to the wafer as photons and the wafer temperature is measured by pyrometry, relying on the correct detection and interpretation of the optical signals from the substrate being processed. Over the past several years, RTP started being used in several low-temperature applications (<700 °C), mostly related to the various metallization processes like source/drain and gate silicidation, and Cu interconnect formation [2]. Although lamp-based annealing is at a disadvantage at these low temperatures – mostly due to pyrometry-related issues [3] and challenges related to the lamp arrays, the use of lamp-based RTP systems is still being promoted even in this low temperature regime. We discuss an alternative way of low-temperature annealing, based on convective and conductive heat transfer to the substrate (a "hot wall" approach) and highlight the fundamental differences between "hot wall" and "cold wall" processes and tools. We demonstrate the suitability of the "hot wall" RTP approach on silicidation examples for Ni and Co.

2. Analysis of low temperature RTP process requirements

The desirable features of a robust and stable annealing process step (most of this list applies to any IC processing step) are as follows:

Repeatability (wafer-to-wafer, between chip layouts, over extended periods of time): Achieving a high degree of repeatability is becoming increasingly important as the overall IC process window is shrinking. Although it is still generally underestimated compared to other process parameters like uniformity, repeatability as a process foundation is increasingly being recognized [4].

Uniformity (within wafer): Without temperature over- or under-shoot, with minimized dependence on the optical properties (both starting and evolving during the annealing process) of the processed substrates. We discuss the so-called pattern effect associated with photon irradiation [5] and challenges with pyrometry-based temperature measurements [3]. One of the most obvious demonstrations of the photon-induced pattern effect is a diffraction pattern. Diffraction is clearly an undesirable artifact for thermal processing, resulting in erratic process behavior with a large degree of complexity and unpredictability.

* Corresponding author. Tel.: +1 408 451 0854; fax: +1 408 451 9279.
E-mail address: igor.malik@wafermasters.com (I.J. Malik).

0167-9317/$ - see front matter
doi:10.1016/j.mee.2007.05.052

Reliability: Resulting from tool and process design considerations, and other practical considerations like energy efficiency, minimized footprint, serviceability, and overall cost of ownership. The simplest possible tool with a minimum of moving parts will best satisfy these requirements.

3. Isothermal cavity annealing systems

We propose to use a "hot wall", near-isothermal cavity for low temperature RTP processing. Fig. 1 shows the basic layout of the stacked annealing oven (SAO) made by WaferMasters, Inc. The SAO can be used for annealing up to 450 °C. The tool has six independently controlled hot plates that form five near-isothermal cavities for wafer processing [6]; the wafer is placed on three quartz standoffs during the processing and is equidistant (~1 cm) from the bottom and top plates. The dominant heat transfer mechanism is convection with a smaller conduction component. The only moving part is the robot. The hot plates are kept at a pre-selected temperature; this arrangement prevents any temperature overshoot. Due to efficient energy coupling between the heat source (the hot plates) and the substrate, the system is highly energy-efficient.

For processes requiring >450 °C temperatures, a single-wafer rapid thermal furnace (SRTF) can be used. As the SAO, it is also essentially an isothermal cavity. It differs from the SAO by having a quartz tube (allowing reactive annealing at temperatures up to 1150 °C) and by having 3 independently controlled temperature zones. Since radiative heat loss from the processed substrates can be signifi-

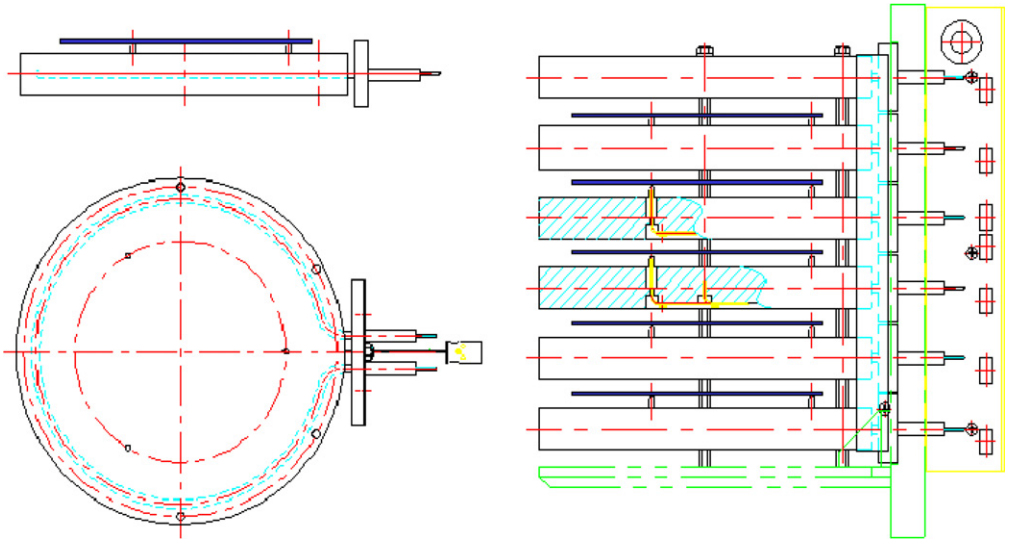

Fig. 1. The schematic of the stacked annealing oven (SAO) RTP tool designed for thermal processing up to 450 °C. Six resistively-heated hot plates with circular footprint form five near-isothermal cavities for wafer thermal processing.

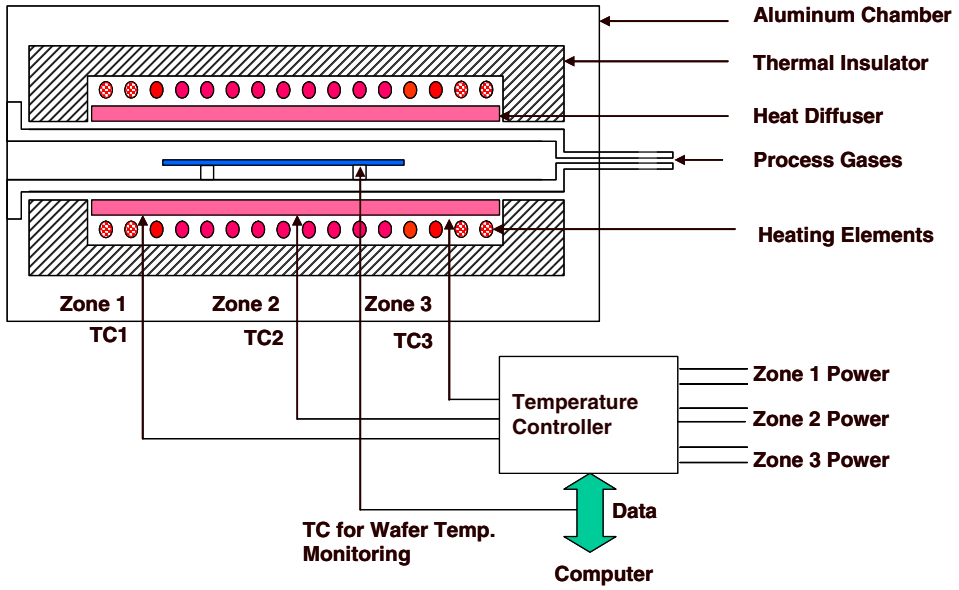

Fig. 2. The schematic of the single-wafer rapid thermal furnace (SRTF) RTP tool designed for thermal processing up to 1150 °C.