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Impact of line-edge roughness on resistance and capacitance of scaled interconnects

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Abstract

The impact of line-edge roughness (LER) on resistance R and capacitance C of on-chip interconnects is for the first time evaluated by a simulation methodology based on a realistic modeling of LER. The model can be calibrated with measured LER parameters. A geometrical approximations of LER is generated and superimposed to an interconnect architecture model with no roughness; resistance and capacitance are extracted from the model by a 3D static solver to estimate the impact of LER on them. By applying this methodology to the interconnect scaling scenario of the 2005 ITRS Roadmap, a small but increasing detrimental effect of LER on both R and C is predicted.

Keywords: Interconnect resistance and capacitance; Line edge roughness; Technology scaling

1. Introduction

Line-edge roughness (LER) and the consequent line-width roughness (LWR) have been mostly studied on polysilicon gates of CMOS transistor. Their impact on transistor parameters has been extensively evaluated [1,5] and it results in degrading device performance and matching.

The impact of LER on interconnects has been rarely reported so far; attempts to introduce artificial periodic square-shaped LER in narrow Cu wire test structures have apparently lead to a decrease in the effective resistivity of the wire or, at least, not to a worsening of the resistivity increase due to the electron scattering [2], which typically affects wires with cross-sectional dimensions below 100 nm.

The mentioned results are based on artificial LER far from being stochastic and depend on an indirect measurement methodology to extract the resistivity, which could be affected by artifacts. The aim of this work is to propose a simulation methodology based on a truly stochastic LER model to be used with a static solver of Poisson and Laplace equations of electrostatics, to directly evaluate the impact of LER on both resistance and capacitance of wires, extending the analysis to the ITRS scaling scenario.

2. LER characteristics

LER is generated during poly and metal patterning process and is due to different causes, including the chemical properties of resist [3,4]. It consists of random-placed nanometer-scale notches and protrusions in the side edges of the patterned line, and feature spatial periodic properties. LER can be characterized by three parameters, namely the absolute roughness amplitude, equal to $3\sigma_{LER}$, the correlation length Λ equal the lowest frequency of the LER amplitude spectrum, and the roughness index α, which describes the frequency content of the spectrum. LER translates into a random variation of the wire width along its length, the line-width roughness (LWR). Since the LERs at the two edges are almost uncorrelated, the relationship between LER and LWR amplitude is $\sigma^2_{LWR} = 2\sigma^2_{LER}$; the other two parameters remain the same.

A LER-affected wire, characterized by an average width w_{AVG}, is intuitively supposed to feature higher resistance

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and capacitance with respect to a wire with no LER and width equal to w_{AVG}. In fact, for the resistance, the effects of small protrusions and notches are not balanced: the enlarged wire cross-section due to the protrusion will not be entirely crossed by the current entering from the adjacent smaller cross-section, present for the statistical alternance of notches and protrusions in LER. Additionally, the notches will restrict the wire cross-section and will increase the local resistance proportionally to their amplitude. Therefore, the effect on R increase of notches is more pronounced than the reduction effect of the protrusions. Similarly, for wire capacitance the 1/spacing dependency of the parallel plate component vs. other parallel wires enhances the contribution to C of places where protrusions of different wires face each other, with respect to the reduction of C in places where the notches are in front of each other.

3. LER model

A model of interconnect affected by LER has been created by starting from the approach presented by Asenov et al. [5] to model LER in poly gates of transistors. In that paper, LER is approximated by a discrete random sequence of roughness amplitudes, obtained by the inverse Fourier transform of exponential or Gaussian approximations of the measured autocovariance function of the LER amplitude vs. distance along the gate or wire length; as such, this sequence preserves the frequency spectrum, the amplitude and the roughness index of the measured LER. This sequence is then used to add roughness to an ideal interconnect architecture model with no LER, composed of a central wire surrounded by two identical coplanar wires and by a top and a bottom plane. This ideal interconnect model is commonly used to extract wire capacitance and resistance by a static solver, namely Raphael 3D by Synopsys [6] and is fully characterized by geometry dimensions as wire width, length, spacing, thickness and by material properties as effective wire resistivity ρ_{eff} and effective

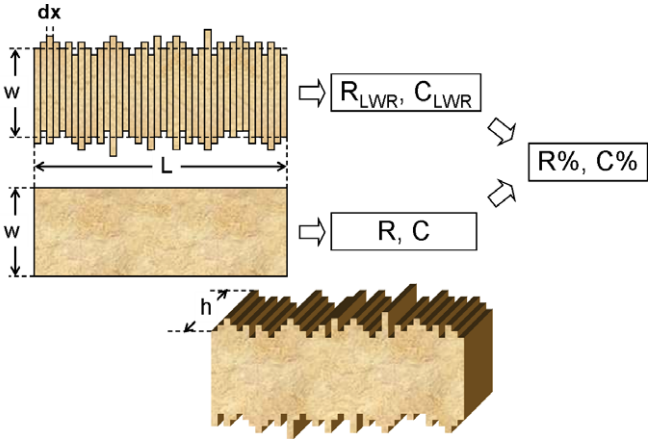

Fig. 1. Simulation approach to extract the increase of R and C due to LER on interconnects.

Table 1
Simulation results of different models of LER impact on DC electrical characteristics of a narrow interconnect

w/s = 20 nm; $L = 18$ nm; $H = 40$ nm; $3\sigma_{LER} = 5$ nm; $A = 20$ nm

	Rectangular	Trapezoidal	Triangular	Gaussian	Exponential
					
R%	6.68	4.16	2.73	1.64	3.08
C%	7.93	3.12	2.08	1.77	3.11
RC%	15.14	7.42	4.86	3.45	6.28