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MOSFET output characteristics after oxide breakdown

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Abstract

The performance of nMOSFETs after the gate oxide (SiO_2) dielectric breakdown (BD) has been studied. Different BD hardness, BD path locations along the channel and device aspect ratios have been considered. The results show that the BD of the gate oxide affects the overall I_D–V_{DS} characteristics and that the BD impact depends on BD hardness and location and device geometry. To describe the post-BD data, a simple BD MOSFET model has been used, which accounts for the after BD additional gate current and drain current effects. The model is able to fit all the observed post-BD behaviours and can be easily included in a circuit simulator, to evaluate the impact of device BD on the post-BD performance of circuits.

Keywords: Dielectric breakdown; Oxide reliability; Leakage currents; Oxide breakdown; Hard breakdown; MOSFET; CMOS; Circuit simulation

1. Introduction

The aggressive size scaling of semiconductor devices has made necessary to pay a special attention to the reliability (dielectric breakdown, BD) of the gate oxide (SiO_2) as one of the causes that can limit the future IC dimensions reduction [1]. The general approach for gate oxide reliability evaluation is based on the study of the gate current, to develop device reliability prediction methodologies since, until recently, the failure of the circuit was considered to be associated to the failure of the device. However, some authors have claimed for a relaxation of the dielectric reliability specifications showing that even after several hard breakdown events (HBD) certain digital circuits can still remain functional [2]. Therefore, for circuit reliability assessment, the impact of BD on the MOSFET drain current will be also critical.

Simulation tools would be useful to evaluate the influence of gate oxide BD on circuit performance. For these simulations, models for the post-BD MOSFET performance are required. Up to now, two different modelling approaches have been adopted. The first one consists in the development of post-BD electrical equivalent circuits for the device. Equivalent electrical circuits for FETs broken down at different positions of the channel have been already presented, which can be included in SPICE simulators [2,3]. In these cases, different equivalent circuits are needed, depending on the BD hardness and BD path position along the channel. Moreover, only the additional BD leakage through the gate is considered, whereas the possible effects of BD on other device parameters are neglected [4,5]. An alternative approach for the post-BD circuit simulation is the description of the broken down MOSFET using models like, for example, BSIM, whose parameters are extracted after the oxide BD [6]. This approach would be the most accurate, but a large number of parameters and a complex extraction process are required.

In this work, the impact of BD hardness, BD path location along the channel and device aspect ratio in the output characteristics of nMOSFETs has been addressed. The results show that the drain current is strongly affected by these parameters. The I_D–V_{DS} curves have been fitted to a simple BD MOSFET model. The model, which can be easily introduced into a circuit simulator, by combining the equivalent circuit definition and parameter extraction

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approaches accounts for the additional leakage current through the gate and the variation of the drain current. The model is able to fit all the measured output characteristics, showing that the post-BD gate current and the variation of the device parameters must be simultaneously considered to get accurate reliability circuit simulations.

2. Experimental

nMOSFETs (1.5 V bulk technology) have been studied. The gate oxide, pure SiO_2 in this work, was 2 nm thick. Transistors with two channel lengths have been considered: short channel devices (aspect ratio 20 μm/0.6 μm) and long channel devices (aspect ratio 20 μm/10 μm). 74 transistors, from which 38 correspond to short and 36 to long channel devices, have been analyzed. Constant voltage stresses (CVS) between 3 and 3.5 V were applied to their gate, with the other terminals grounded to provoke oxide BD. The gate (I_G), drain (I_D) and source (I_S) currents through the transistor as a function of the gate voltage, V_G, and also the I_D–V_{DS} characteristics have been measured before and after BD. The samples have been classified in 3 groups depending on the BD path location along the channel: channel BD, when the BD is located between gate and channel, drain BD, when the BD path is located between gate and drain overlap region, and source BD, when it is located between gate and source overlap region. The BD path position along the channel has been determined by measuring I_D and I_S for $V_G = -1.5$ V (MOSFET in accumulation) and evaluating the ratio $I_D/I_D + I_S$, following the standard procedure presented in [7]. This ratio will be close to 0 or 1 depending on whether most of the injected electrons through the breakdown path are collected at the source or drain terminals, respectively, so that it can be used to distinguish between source, channel or drain breakdown. Due to the symmetry of the stress (source and drain were grounded), the BD occurrence along the channel is equiprobable. However, in the whole set of devices, 47 experienced a BD in the drain, 22 in the source and 5 in the channel. This BD distribution is compatible with other tendencies reported before [7]. Isolated transistors are studied, which corresponds to the worst case (load/driving effects which can limit the BD hardness when the device is within a circuit [8] are not considered).

3. Oxide breakdown effects on nMOSFETS output characteristics

In this section, the impact of BD on the I_D–V_{DS} characteristics will be studied, by comparing the pre and post-BD curves measured in the transistors. Soft and hard breakdown (progressive BD [9] is not considered in this work), BD path position along the channel and transistor geometry have been considered for the case of nMOSFETs. Figs. 1–3a show typical post-BD I_G–V_G curves measured on the devices (fresh curves are included for comparison), which are indicative of the BD hardness. I_D–V_G and I_S–V_G curves

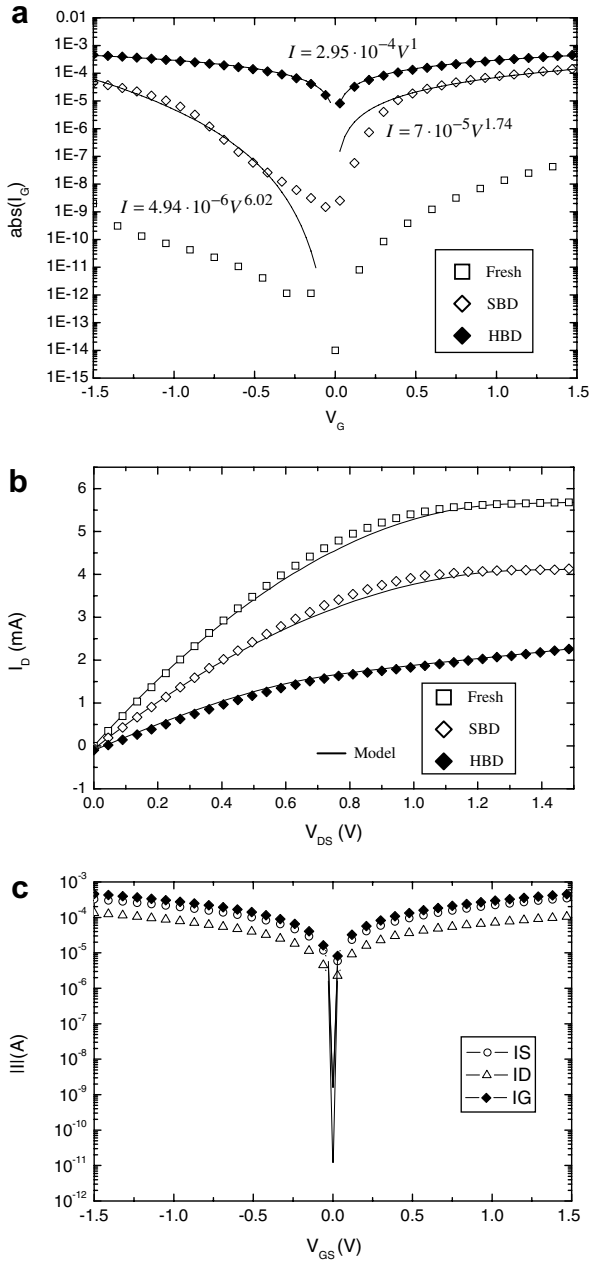

Fig. 1. Typical *I-V* characteristics measured on transistors that suffered SBD (open diamonds) and HBD (solid diamonds) events. BD took place in the channel ($L = 0.6$ μm). Fresh characteristics (open squares) are included. (a) I_G–V_G curves, continuous lines correspond to the fitting of the data to a law of the type $I_G = KV_G^p$ (the current dependencies are also specified) (b) I_D–V_{DS} characteristics measured for $V_G = 1.5$ V, continuous lines correspond to the fitting of the data to the BD MOSFET model. (c) Post-BD I_G–V_G, I_S–V_G and I_D–V_G curves for the HBD event in Fig. 1a. These curves are used to determine the BD location.

are used to determine the BD path location along the channel from the ratio $I_D/I_D + I_S$ [7]. To show an example, in Fig. 1c, the I_S–V_G, I_D–V_D, I_G–V_G curves measured for the HBD event in Fig. 1a are shown. Note that I_D and I_S are lower than I_G for negative VG value, which is interpreted as a BD event in the channel. In this case the ratio $I_D/I_D + I_S = 0.25$ (for $V_G = -1.5$ V), so that the BD path