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Finite-point method for efficient timing characterization of sequential elements

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ABSTRACT

Timing characterization of sequential elements, such as latches and flip-flops, is one of the critical steps for timing closure in the pipelined design. Traditional characterization of setup and hold time constraints is computationally intensive, due to the demand on high accuracy in monitoring the operation failure. To improve the efficiency, this work proposes a finite-point based method for the characterization of setup and hold time constraints. The finite-point method identifies several critical data points in the non-linear curve of timing characteristics, and abstracts the essential setup/hold information from them. Moreover, compact models are derived for each point, further reducing the computation cost. The proposed method is general for all sequential elements in the standard cell library. It is comprehensively validated using benchmark circuits at 45 nm node. Experimental results demonstrate approximately 25 × reduction in characterization time, with the prediction error in setup and hold time within 9% of FO_4 nominal delay, as compared to that of SPICE simulation results.

1. Introduction

The scaling of CMOS technology has led to higher variability in device and circuit performance, causing timing un-certainties in VLSI design. Due to process variations in many device parameters, such as channel length, threshold voltage and gate dielectric thickness, sequential circuit elements have experienced an excessive amount of timing variability in both setup and hold time. Furthermore, dynamic variations, such as the uncertainty due to simultaneous switching in a multiple input gate, may further induce delay variations by more than 16% at 90 nm technology node [1]. As a consequence, the number of setup and hold violations in a synchronous design increases by more than 15% at 45 nm technology node [2]. To ensure correct circuit functionality and performance in this context, accurate timing information of sequential elements, especially on setup and hold time, is one of the crucial steps in library characterization and design closure.

In a traditional static timing analysis (STA) flow that is applied to critical path analysis, the essential timing parameters, such as setup and hold time of a sequential element, are stored in a lookup-table format (LUT) [3]. Such lookup-table models need to be characterized at all process, voltage and temperature (PVT) corners, using worst-case state vectors with dynamic SPICE-level simulations [4–7]. Since the failure criteria of a sequential element are highly non-linear and sensitive to process and design conditions, very detailed SPICE simulations are required and thus, the computation cost is high [8]. As the technology scales and the number of PVT corners are rapidly increasing, even the binary search method suffers from a significant computation cost and data volume, as presented in Table 1. The situation is further exacerbated when statistical timing analysis becomes a must at advanced technology nodes. As compared to corner based analysis, statistical STA demands much more sampling points and increases the computation cost [6–7].

Various techniques have been developed to reduce the pessimism of setup and hold time characterization in STA [8–10]. For instance, Reference [9] exploits the failure criteria of setup time in the STA. Using the interdependent behavior of setup and hold times [8], a numerical algorithm is studied for independent and correlated setup and hold time characterization. In this work, we further propose a model based solution to characterize the timing metrics of sequential elements, with much higher computation efficiency and without sacrificing the accuracy.

Fig. 1 illustrates the basic idea. It shows a representative timing curve, such as T_{D2Q} vs. T_{D2CLK} of a latch [11], for setup time characterization. Here T_{D2Q} is the propagation delay from data input (D) to data output (Q) of the latch when the latch is transparent and T_{D2CLK} is the setup time of D with respect to clock (CLK). Due to the level sensitive behavior of the latch, the propagation delay is measured from D to Q (T_{D2Q}) for a given setup time or hold time, when the latch is transparent. Where as in the case of flip-flop, due

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Table 1
Dynamic latch: computation cost for setup and hold time at various PVT corners at 45 nm node

$\tau_{CLK} \times \tau_D \times C_L$ (LUT)[a]	Normalized to mid-point $\tau_{CLK} \times \tau_D \times C_L$ (TT) PVT Corners[b]		
	TT	TT+SS+FF	TT+SS+FF+FS+SF
$1 \times 1 \times 1$	1	3	5
$5 \times 5 \times 5$	125	375	625
$7 \times 7 \times 7$	343	1029	1715
$10 \times 10 \times 10$	1000	3000	5000

Step size of SPICE simulation=2.5 ps
LUT: lookup-tables in the library model;

[a] τ_{CLK} ,τ_D: input transition time for clock and data; C_L: output fanout.
[b] TT: typical corner; SS: slow-slow corner; FF: fast-fast corner.

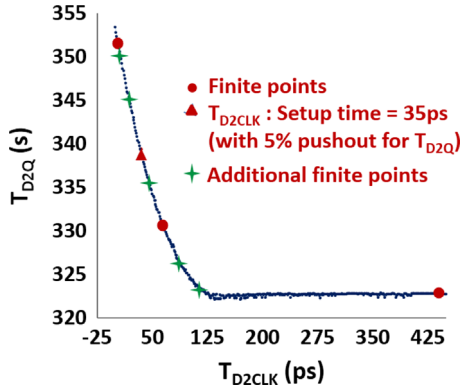

Fig. 1. The concept of finite-point based characterization for the nonlinear behavior of setup and hold time of sequential elements.

to edge sensitive behavior, the propagation delay is measured from from *CLK* to *Q* (T_{CLK2Q}) for a specific setup time or hold time respectively. In the case of hold time characterization the curve in Fig. 1 will be represented as T_{D2Q} vs. T_{CLK2D}, where T_{CLK2D} is the hold time of *D* with respect to *CLK* for a latch. The delay keeps constant when there is sufficient separation between data and clock arrival time. However, as the interaction between data and clock becomes stronger, the delay rapidly increases and eventually fails the operation. This behavior is general for many types of sequential element design. Although the exact curve depends on the circuit topology, such a curve can be bounded by two linear lines, defined by minimum of three finite points shown in Fig. 1. Their slope and the cross point will capture the essential timing characteristics.

Based on this observation, our work introduces an abstract approach, in which a finite number of points are used to describe the non-linear timing curve in Fig. 1. The typical number of points are three in order to define two lines in Fig. 1. After a robust definition of these critical finite points are available, compact timing models are further derived for each point, achieving high efficiency in the extraction of setup and hold time. The idea behind this finite point based approach for sequential cell characterization is to simplify the VLSI design flow. During the initial phase of the design, the preliminary design and fine tuning of the sequential element itself is happening at circuit/device level. The VLSI design flow and methodology is highly dependent on the fundamental elements such as combination and sequential elements. Thus the finite point based characterization approach helps initiate the top down approach. Such parallel effort avoids dependencies in the VLSI design and helps identify the issues with design flow ahead of time prior to final design closure. This characterization approach is generic for different types of sequential elements. The finite points are the SPICE simulated delay for a specific setup or hold time of the circuit, which captures the device and circuit level behaviors. Thus accurately identifying the finite points per circuit behavior is the critical step to this characterization approach. The finite point characterization approach ensures that the finite points in Fig. 1 are defined in such a way that the sequential cell behavior for the critical point is captured before the circuit enters the failure state. Further, the accuracy of the finite point model can be improved with few additional points as shown in Fig. 1 with some additional computation cost. Thus, the meta-stability [12] is bypassed in this characterization method. This simplified approximation is valid as the variability in modern technology is accounted by applying additional margin to account for process variation.

Section 2 presents the definition of finite points, the terminology, modeling principles and procedures applied to finite-point characterization. A dynamic latch is used for the demonstration. In Section 3, the proposed characterization methodology is extensively validated with nominal SPICE simulations at the 45 nm technology node, for various sequential elements in the standard cell library. To be realistic, the validation is based on post-layout SPICE netlist from 45 nm NANGATE library [13]. Interconnect parasitic are calculated from Predictive Technology Model (PTM) [14]. A realistic input waveform is generated from a CMOS gate driver, and active CMOS gate load with different fan-out (FO) numbers is used at the output. Furthermore, Section 3 demonstrates the new characterization methodology at fast and slow operating conditions for a wide range of input transition time for clock and data inputs, and for various output load conditions. Section 4 summarizes this work.

2. Model development

2.1. Modeling strategy of the finite-point approach

The finite-point model is derived from the fundamental behavior of a sequential element, such as a latch or a flip-flop. Without losing the generality, active high dynamic latch is used in this section to explain the concepts. The schematic is shown in Fig. 2. Setup time is defined as the time interval before the active clock, when the data must be stable to meet the performance requirement of the design. Whereas the hold time is the time interval after the active clock edge where the data must be held stable to meet the desired functionality of the design. In general, the setup and hold time behavior of a dynamic latch is as shown in Fig. 2 and Fig. 3, respectively. For a simplified approximation, T_{D2Q} versus the setup time (T_{D2CLK}) or hold time (T_{CLK2D}) curve can be constructed using three finite points A, B, C as marked in Figs. 2 and 3, respectively.

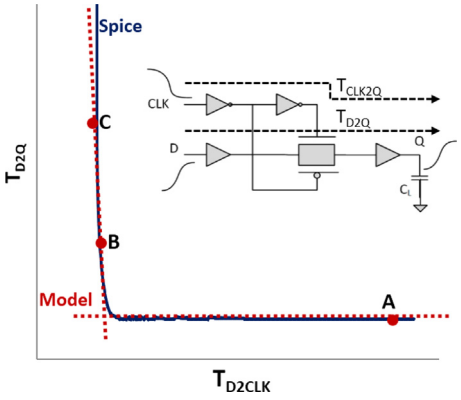

Fig. 2. Setup time characteristic of a dynamic latch with three points used for finite-point based characterization model.