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Enhancement of test data compression with multistage encoding

S. Sivanantham [a], M. Padmavathy [b], Ganga Gopakumar [c], P.S. Mallick [a,*], J. Raja Paul Perinbam [d]

[a] School of Electrical Engineering, VIT University, Vellore 632014, Tamil Nadu, India
[b] School of Electronics Engineering, VIT University, Vellore 632014, Tamil Nadu, India
[c] Sankalp and KPIT Semiconductors Pvt. Ltd, Bangalore, Karnataka, India
[d] Department of ECE, KCG College of Technology, Chennai 600097, Tamil Nadu, India

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ABSTRACT

In this paper, we present two multistage compression techniques to reduce the test data volume in scan test applications. We have proposed two encoding schemes namely alternating frequency-directed equal-run-length (AFDER) coding and run-length based Huffman coding (RLHC). These encoding schemes together with the nine-coded compression technique enhance the test data compression ratio. In the first stage, the pre-generated test cubes with unspecified bits are encoded using the nine-coded compression scheme. Later, the proposed encoding schemes exploit the properties of compressed data to enhance the test data compression. This multistage compression is effective especially when the percentage of do not cares in a test set is very high. We also present the simple decoder architecture to decode the original data. The experimental results obtained from ISCAS′89 benchmark circuits confirm the average compression ratio of 74.2% and 77.5% with the proposed 9C-AFDER and 9C-RLHC schemes respectively.

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1. Introduction

Developments in process technology have led to the design of systems with millions of transistors on a single chip and it has resulted in an increase of test data required to test the circuits. Conventional external testing processes involve storing all test vectors and test responses on the automatic test equipment (ATE) memory. The test data volume for the scan-based test is normally very large due to its single pattern length generated using a combinational automatic test pattern generation (ATPG) tool. The test application time depends on the amount of test data stored on ATE, the time required to transfer the test data from ATE to the core and length of the scan chain. But these testers have limited memory, speed and I/O channels. The system-on-a-chip (SoC) revolution also gives challenges in the area of power dissipation, especially for design and test engineers. Generally, a circuit or system consumes more power in a test mode than in a normal mode. This high power consumption during testing affects the circuit reliability [1]. Test power depends on the number of scan elements present in the circuit. Efficient test data reduction techniques can reduce the testing time, test power and ATE memory requirements.

Linear compression schemes are very efficient at exploiting unspecified bits in the test cubes to achieve a large amount of compression. Several on-chip pattern decompression techniques were proposed to reduce test data volume such as linear feedback shift register (LFSR) reseeding [2–6], mutation encoding [7], scan-chain concealment [8], reconfigurable serial multiplier [9], packet-based compression [10] techniques are among these categories. A scan architecture called reconfigured scan forest was proposed to reduce test data volume and test application cost by [11]. Ward et al. [12] proposed a scheme which combines a linear decompressor with a non-linear decoder to provide very high levels of compression for test data. A technique for simultaneous reduction of both test data volume and test power named linear decompressor based test compression is presented in [13]. This scheme divides the test cubes into two blocks, namely test cube with low toggles and high toggles which feeds the scan-chain with a novel design-for-testability (DFT) architecture to reduce the scan-in transitions. Several other techniques such as embedded deterministic test (EDT) [14], smartBIST [15] and reconfigurable interconnection network (RIN) [16] were also proposed to reduce the test data volume. However, these methods are not suitable to test the embedded cores since structural information of the circuits is required for test generation and fault simulation. Test data compression based on time-multiplexing is presented in [17],

* Corresponding author.
E-mail addresses: ssivanantham@vit.ac.in (S. Sivanantham), psmallick@vit.ac.in (P.S. Mallick).

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where the compressed seeds are passed to every embedded core by sharing the data channels. Solana [18] proposed a new scan architecture called virtual chain partition (VCP), which is useful for embedded cores to reduce the test application time, test data volume and test power. This scheme determines the maximum reduction in test cycles obtainable with the architecture and selects the most suitable configuration for each circuit. However, this scheme requires large area overhead.

The code-based schemes use data compression techniques such as statistical coding [19,20], Golomb coding [21] and run-length coding [22–30] to encode the test cubes. In these approaches, the original data are partitioned into symbols, and then each symbol is assigned to a codeword to form the encoded data. Each codeword is converted into the corresponding symbol with on-chip decompression hardware. These methods do not require the structural information about the circuit under tests (CUTs) and they are more suitable for intellectual property (IP) core based SoCs. Tehranipoor et al. [31] proposed to use only nine codewords to encode the test data. The frequency-directed run-length (FDR) code [30] is a variable-to-variable-length code which maps variable-length runs of 0 s to variable-length codewords. The FDR code is not suitable for the test sets which contains more number of 1 s. The compression methods such as alternating FDR (ALT-FDR) coding [23], extended FDR (EFDR) coding [24], alternating variable-length (AVR) coding [25], equal-run-length coding (ERLC) [26], shifted FDR (SFDR) coding [27] and modified FDR (MFDR) coding [28] consider both runs of 0 s and 1 s to form the codewords. Rosinger et al. [29] presented a minimum transition count (MTC) filling approach for simultaneous reduction of test data volume and power dissipation.

Statistical codes form the variable-length codewords for fixed-length of data blocks. Among the available statistical codes, Huffman code [32] provided a good compression efficiency because of its shortest average codeword length. The Huffman coding technique with fixed-length of blocks to reduce the test data volume is described in [19]. However, it requires complex decoder architecture to decode the large number of distinct blocks. Several Huffman based compression techniques such as variable-input Huffman coding [33], variable-to-variable Huffman coding [34], selective Huffman coding [35], optimal selective Huffman coding [36], complementary Huffman coding [37] and modified selective Huffman coding [38] are proposed to improve compression efficiency, area overhead and test application time. The technique exploits reordering of test patterns to minimize the shapes needed to encode the test data which is presented in [39]. Compression of the test data by geometric shapes is described in [39]. A technique based on merging consecutive compatible blocks of the test data is presented in [40]. Wolff et al. [41] proposed to use a popular software compression algorithm called LZ77 to reduce the test data volume. A method which iteratively encodes $2^{|n|}$ runs of compatible or inversely compatible patterns into a codeword is presented in [42].

Many code-based compression techniques have the objective of only reducing the test data volume without emphasis on test power reductions. For example, the compression techniques described in [24,31,33–36,43,44] focus mainly to reduce the test data volume. Several test independent compression techniques were used to reduce the test power and test data volume [24–26,45]. The zero-fill algorithm is used in [30,44] to maximize the 0-runs to reduce scan-in test power. The zero-fill algorithm fills the unspecified bits with 0 s. The X-bits are filled with 0 s or 1 s in order to improve skewing of the occurrence frequencies of the distinct blocks [35,43]. In ALT-FDR coding, all unspecified bits are filled to minimize the weighted transition metric (WTM) [23]. The ALT-FDR also reports a significant reduction in scan-out phase, but achieves less compression ratio since the unspecified bits are filled to reduce the test power.

Many authors gave their attention to multistage test data compression techniques to enhance the compression ratio. Mixing of run-length encoding and Huffman coding techniques to reduce the test data volume, test power and test application time is described in [45]. Lingappan et al. [46] presented multilevel compression techniques where the test data is compressed using the Huffman coding/embedded deterministic test technique and the compressed test set is further compressed using the LZ77 technique. The compression technique described in [43] uses multilevel Huffman coding to improve the compression ratio. Several hybrid test data compression/decompression schemes are presented in [47–49]. A technique to compress/decompress the test data using cyclical de-compressors and run-length coding is described in [47]. Most of the low-power compression techniques do not address the test power reduction in scan-out phase.

1.1. Main contribution

We present two multistage compression techniques called 9C-AFDER and 9C-RLHC to achieve high compression ratio, low scan-in and scan-out test power with small area overhead. To accomplish these objectives, we present two encoding methods, one is based on run-length coding and another is based on Huffman coding. Both the methods exploit the properties of encoded test obtained from 9C compression to enhance the compression ratio. First the test set with unspecified bits is compressed with the nine-coded compression technique and the resultant test set is further encoded with proposed alternating frequency-directed equal-run-length coding (AFDER) or run-length based Huffman coding (RLHC) schemes. The remaining unspecified bits in the 9C encoded test sets are filled with logic values to reduce test power. We also present the decompression architecture to decode the encoded test which will take small area overhead and overall test application time.

In Section 2, we describe the motivation behind this work and review the nine-coded compression technique. Then we describe our proposed encoding schemes with examples. Section 3 describes the decompression architectures, Section 4 presents the experimental results obtained for the proposed compression schemes, and Section 5 concludes.

2. Multistage encoding techniques

2.1. Motivation

The ATPG generated test cube to test the typical industrial circuits normally contain 95–98% of unspecified bits [15]. These bits can be freely filled with the logic values (0 or 1) in order to reduce the test data volume and/or the test power. However, filling of X-bits to reduce the test data volume may increase the test power or vice versa.

In the nine-coded compression technique [31], the unspecified bits in the test cubes were utilized in order to achieve better compression ratio. The compressed data still contain a large number of unspecified bits. These unspecified bits can be filled to reduce the test power without compromising the compression ratio. One interesting property observed with this method is that, it also provides better power reduction in test applications. To the best of our knowledge, this inherent property of test power reductions in the 9C technique was never reported in the literature so far. The encoded test set obtained from 9C coding consists of long runs of 0 s and 1 s, as well as a large number of repeated codewords can also be noted. For example, the circuit s13207 has 1423 runs of 0 s, 1947 runs of 1 s and 346 consecutive equal-runs. Hence, the encoded test volume can be further reduced by

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