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Compact model to efficiently characterize TSV-to-transistor noise coupling in 3D ICs ☆

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ABSTRACT

A methodology is proposed to characterize through silicon via (TSV) induced noise coupling in three-dimensional (3D) integrated circuits. Different substrate biasing schemes (such as a single substrate contact versus regularly placed substrate contacts) and TSV fabrication methods (such as via-first and via-last) are considered. A compact π model is proposed to efficiently estimate the coupling noise at a victim transistor. Each admittance within the compact model is approximated with a closed-form expression consisting of logarithmic functions. The methodology is validated using the 3D transmission line matrix (TLM) method, demonstrating, on average, 4.8% error. The compact model and the closed-form expressions are utilized to better understand TSV induced noise as a function of multiple parameters such as TSV type, placement of substrate contacts, signal slew rate and voltage swing. The effect of differential TSV signaling is also investigated. Design guidelines are developed based on these results.

1. Introduction

Three-dimensional (3D) integrated circuits (ICs) have emerged as an effective solution to some of the critical issues encountered in 2D ICs such as the adverse effects of global interconnects [1,2]. In wafer-level 3D technologies, multiple wafers are thinned, aligned, and vertically stacked. For example, alignment accuracy of 1 μm has already been demonstrated [3]. Multiple bonding techniques have also been developed such as adhesive [4,5], oxide [6], and metal bonding [7]. The wafer thinning capability varies from hundreds of nanometers to several hundred micrometers, depending upon whether bulk silicon or silicon-on-insulator technology is utilized [8,9].

Through silicon vias (TSVs) provide communication among different tiers of a 3D stack, reducing the global interconnect length [2]. Several distinct TSV fabrication methods exist depending upon when the TSVs are formed. These methods are (1) via-first/middle [10,11] and (2) via-last TSVs [12]. Furthermore, since the tiers can be separately processed using different technologies, heterogeneous integration of diverse circuits and materials is facilitated, as depicted in Fig. 1.

International Technology Roadmap for Semiconductors identifies three phases for the application of 3D integration technology: (1) memory stacks, (2) processor-memory stacks, and (3) heterogeneous 3D integration with sensing and communication blocks [13]. An important challenge in each of these applications is to ensure system-wide signal integrity, which is exacerbated due to the multiple tiers interconnected with TSVs. In addition to traditional noise coupling and propagation mechanisms such as cross-talk, power supply noise, and substrate coupling, 3D ICs suffer from TSV induced noise coupling [14,15]. Specifically, during a signal transition within a TSV, noise couples from TSV into the substrate due to both dielectric and depletion capacitances. The coupling noise propagates throughout the substrate and affects the reliability of nearby transistors. This issue is exacerbated for TSVs that carry signals with high switching activity factors and fast transitions such as clock signals.

Analog/RF blocks and memory cells are among the most sensitive circuits to substrate noise coupling. For example, in [16], experimental data demonstrates that the signal-to-noise-plus-distortion ratio (SNDR) of a delta-sigma modulator is reduced by more than 20 dB due to substrate noise. Note that in heterogeneous 3D systems (see Fig. 1), the front-end circuitry consisting of analog/RF blocks is typically located at the top plane (closer to the I/O pads) to reduce the overall impedance between the pads and analog inputs. In this floorplan, TSVs are required to transmit the digital signals (including the clock signal) to the data processing plane. Thus, TSV induced noise becomes an important issue

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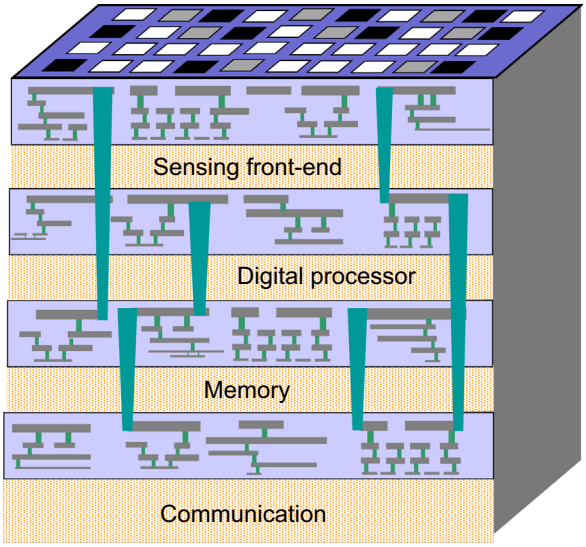

Fig. 1. Three-dimensional integration of diverse planes using through silicon via technology [2].

for the reliability of the analog/RF blocks. Digital transistors are also affected by TSV induced noise if the physical distance between the TSV and device is sufficiently short [17]. TSV induced noise changes the drain current characteristics of both an on and off transistor, as observed in [18].

Existing works have investigated TSV induced noise coupling using different approaches [19,20]. For example, in [19], the effect of several parameters such as substrate type, TSV height, TSV isolation layer thickness, transient signal slew rate has been investigated. An *RC* grid has been used to model the substrate. Alternatively, some works have focused on the mitigation of TSV induced noise. In [20], the efficacy of traditional techniques (such as guard rings) in reducing TSV induced noise has been investigated. A three-dimensional transmission line matrix (3D-TLM) method has been used to model the TSVs and substrate. These studies, however, do not consider different substrate biasing schemes and distinct TSV fabrication methods. Furthermore, computationally expensive approaches (such as 3D-TLM and field solvers) are utilized, prohibiting the use of these approaches for fast evaluation of different physical structures during the early stages of TSV floorplanning.

The primary contributions of this paper are as follows: (1) a compact model and a closed-form expression for each parameter within this model are developed to efficiently estimate TSV induced noise at a victim transistor, (2) the effect of different substrate biasing schemes and both via-first and via-last TSV characteristics are considered by the proposed model, which is validated using the 3D-TLM method, (3) design guidelines on substrate contact placement, TSV type, slew rate and voltage swing of the transient signals, and differential signaling are provided to reduce TSV induced noise based on the results obtained from the proposed compact model.

The rest of the paper is organized as follows. A highly distributed electrical model (used as a reference to validate the proposed compact model) to analyze noise injection and propagation is described in Section 2. A compact π model is proposed in Section 3 for efficient estimation of TSV induced noise at a victim transistor. Each admittance within the compact model is expressed in Section 4 as a function of multiple physical parameters. This approach is useful to consider different substrate biasing schemes and TSV types. Design guidelines are provided in Section 5 based on the analysis results obtained from the compact model. Finally, the paper is concluded in Section 6.

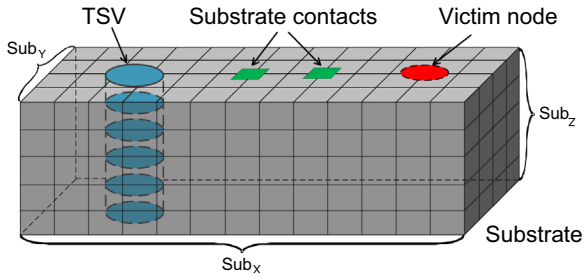

Fig. 2. Physical structure used to analyze TSV induced noise coupling.

2. Distributed model for TSV induced noise coupling

To characterize TSV induced noise coupling as a function of multiple design parameters, the physical structure depicted in Fig. 2 is used. This structure consists of a noise injector (TSV), a noise transmitter (substrate), and a noise receptor (victim transistor). Substrate contacts are also included to bias the substrate. Note that the number and placement of substrate contacts between the TSV and the victim transistor play an important role in the noise coupling analysis and safe zone characterization, as demonstrated in this paper.

To analyze this physical structure, several approaches have been adopted such as using an electromagnetic field solver, a device simulator, and a highly distributed model using a 3D TLM method [20–22]. In the distributed model, the physical structure is discretized into unit cells (for both TSV and substrate) and each unit cell is modeled with lumped parasitic impedances. A distributed model based on 3D-TLM is described in this section. This model is used as a reference to validate the proposed compact model (see Section 3) and closed-form expressions (see Section 4). The TSV and substrate models are described, respectively, in Sections 2.1 and 2.2. The advantages and limitations of a 3D-TLM based distributed model are discussed in Section 2.3.

2.1. TSV model

A typical TSV is represented as a cylinder with a diameter and depth, as illustrated in Fig. 3(a). Two primary components of a TSV are (1) conductive filling material such as polysilicon, tungsten or copper (varies depending upon the specific TSV fabrication technology as mentioned in Section 2.1.1) and (2) a dielectric layer that surrounds the conductive part to prevent the filling material from diffusing into silicon [12]. Different types of TSVs are summarized in the following section.

2.1.1. Via-first and via-last TSV technologies

TSVs are classified as via-first and via-last depending upon the fabrication method [23]. In the via-first method, TSVs are fabricated before the front-end-of-line (FEOL) process, *i.e.* before the transistors are etched within the silicon substrate. Alternatively, in a via-last technology, the TSVs are manufactured after the back-end-of-line (BEOL) process, *i.e.* after the metalization layers are fabricated.

Via-first TSVs utilize high resistivity polysilicon as the filling material. Polysilicon can withstand high temperatures required during the processing steps [23]. Alternatively, a low resistivity copper is used for via-last TSVs since via-last TSVs are fabricated after the formation of transistors and metal layers [23]. The physical dimensions of the TSVs are also affected by the fabrication