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Designing soft-edge flip-flop-based linear pipelines operating in multiple supply voltage regimes ☆

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ABSTRACT

Soft-edge flip-flop (SEFF) based pipelines can improve the performance and energy efficiency of circuits operating in the super-threshold (supply voltage) regime by enabling the opportunistic time borrowing. The application of this technique to the near-threshold regime of operation, however, faces a significant challenge due to large circuit parameter variations that result from manufacturing process imperfections. In particular, delay lines in SEFFs have to be over-designed to provide larger transparency windows to overcome the variation in path delays, which causes them to consume more power. To address this issue, this paper presents a novel way of designing delay lines in SEFFs to have a large enough transparency window size and low power consumption. Two types of linear pipeline design problems using the SEFFs are formulated and solved: (1) designing energy-delay optimal pipelines for the general usage that requires SEFFs to operate in both the near-threshold and super-threshold regimes, and (2) designing minimum energy consumed pipelines for particular use case with a minimum operating frequency constraint. Design methods are presented to derive requisite pipeline design parameters (i.e., depth and sizing of delay lines in SEFFs) and operating conditions (i.e., supply voltage and operating frequency of the design) in presence of process-induced variations. HSPICE simulation results using ISCAS benchmarks demonstrate the efficacy of the presented design methods.

1. Introduction

With the increase in demand for battery-powered devices and mobile equipment, the need for energy-efficient designs gains growing attentions. The ultra-low voltage operation, in particular, *near-threshold* (NT) operation, is quite effective in minimizing the energy consumption of a design by reducing its supply voltage to a level close to the threshold voltage of the transistors, V_{th}. Indeed, previous work on NT operation proved the existence of and analytically derived the *minimum energy* (*operation*) *point* (MEP), which is the optimal supply voltage level that minimizes the energy consumption [2,3]. However, NT operation comes at the cost of sacrificing the circuits' timing performance [4,5]. Hence, it is especially beneficial for applications that have relaxed timing requirements, e.g., medical monitoring devices and many types of environmental sensors. Note that digital circuits operating in the NT regime become quite sensitive to process-induced variations. For example, in 90 nm CMOS technology, the relative delay variation, defined as $3\sigma/\mu$, of a combinational logic block operating at 0.5 V increases by 2.5X compared to that of a block operating at 1 V [6].

An SEFF is a D flip-flop with an additional *delay line* (DL). The DL is added to postpone clock edges of the master latch to create a *transparency window* during which both master and slave latches are transparent. The transparency window allows the SEFF to pass a positive slack from one pipeline stage to the next. The *transparency window size* is also referred as *softness*. The SEFF-based pipelined circuits improve the operating frequency of the pipeline by enabling time borrowing from the non-critical stages to the critical stage. In addition, process variations are alleviated for "deeper" combinational logics since the local random variation cancel out when the logic depth increases [6,7]. Thus, soft edges between pipeline stages help to reduce the sensitivity of pipelined circuits on process variations.

Thanks to its properties of frequency enhancement and variation tolerance, we bring the SEFF-based pipeline to the NT regime. Precisely, we focus on designing and optimizing SEFF-based linear pipelines operating in multiple supply voltage regimes from the NT to *super-threshold* (ST) in this work. We show that SEFF-based pipelines that are optimized for operations in the ST regime [7,8] are not suitable in the NT regime. In particular, since circuit delays in the NT regime have an exponential relationship with the transistor threshold voltage, the variation in transistor threshold voltage causes a huge amount of variation to the SEFF softness. Therefore, SEFFs designed in [7,8] cannot provide enough softness in the NT regime to deliver a

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certain timing yield. In order to design SEFF-based pipelined circuits that can operate in all supply voltage regimes, the key is to ensure that the same transistor sizes result in effective operation of the DL in all voltage regimes (and hence, appropriate setting of the FF softness) under process-induced variations.

We present a novel way of designing DLs in SEFFs to provide enough softness and reduce their power consumptions. Precisely, we add a PMOS header between the conventional DL and the supply voltage rail. The PMOS header results in a slight supply voltage drop on the DL, which is negligible in the ST regime but has a significant impact on the softness in the NT regime. Along with the increased softness, another benefit is the reduced leakage power consumption of the DL due to the *transistor stack effect*. We formulate the SEFF-based linear pipeline design problems and present methods to derive the optimal design parameters, such as the configuration and sizing of DLs. The presented methods also determine the optimal operating conditions, including the supply voltage and operating frequency, according to the problem setup and pipeline designs.

We solve two SEFF-based linear pipeline design problems. The first problem setup targets pipelined circuits operating in mixed NT and ST regime. We adopt the *energy-delay product* (EDP) as the cost function and minimize the EDP over all supply voltage levels. In particular, we formulate the EDP minimization problem for SEFF-based pipelined circuits as a mathematical programming problem, where the clock period, PMOS header width, and configurations of delay lines are optimization variables. The second problem targets the situation in which target pipelined circuits are required to meet some pre-specified minimum operating frequency. Since the frequency is constrained by the problem setup, we adopt the total energy consumption in one clock cycle as the cost function. We find the MEP and corresponding pipeline design parameters that satisfy the frequency constraints. The timing constraints of pipelined circuits are imposed by using the 3σ delay and accounting for the delay variation from every circuit component. We generate fitted Pareto-optimal lines of the DL between energy/power consumptions and FF softness so that we can select the DL configuration and sizing solution that are closest to optimal ones. Experimental results based on ISCAS benchmarks show significant reduction of up to 18.4% in EDP for the first problem and 9.1% in energy consumption for the second problem, respectively.

The remainder of the paper is organized as follows. The notion of SEFF-based pipelined circuits is reviewed in Section 2. In Section 3, we discuss design challenges in the NT regime and provide a novel way of designing DLs so that we can better apply the SEFF-based pipelining technique in the NT regime. We formulate two versions of the SEFF-based pipeline design problem and present solution methods for these in Section 4. Finally, experimental results are presented in Section 5.

2. Background

SEFF-based pipelines are capable to combat process variations and improve the timing performance of pipelined circuits. This section starts off by reviewing the related work, and continues by explaining how SEFFs enable opportunistic time borrowing across pipeline stages and presenting setup and hold timing conditions in a SEFF-based pipeline. Finally the energy-delay product is proposed as the metric to use in order to quantify the performance of pipelined circuits.

2.1. Related work

Pipelining is a well-known technique to improve the timing performance and energy efficiency of the processor [9]. Considerable efforts have been invested to design energy-efficient pipelined circuits. Jacobson in [10] presented clock-gating technique to reduce the power consumption of a microprocessor pipeline. Kim in [11] combined pipelining and parallel processing to reduce power consumption by 40%. Srinivasan in [12] investigated the optimal pipeline depth to balance the power consumption and timing performance. However, none of these work focused on the ultra-low voltage operation regime, which requires special techniques to handle process variations. Recently, authors in [13] explored aggressive latch-based super-pipelining technique and demonstrated the energy efficiency improvements for a 65 nm FFT core operating in ultra-low voltage regime. Although the latch-based pipeline design shows good capability of handling process-induced variations, it has many limitations including hold time violation issues, design difficulties using standard EDA tools, and the requirement of an extra clock network, which makes it power and area inefficient.

Applying soft-edge flip-flops (SEFFs) to digital circuits is a useful technique to improve the circuit performance. Joshi [7] presented to utilize SEFFs in sequential circuits to increase the timing yield in the presence of process variation. Authors in [14] adopted SEFFs to combat delay variations caused by NBTI. Authors in [8 and 15] presented an SEFF-based pipeline design method that utilizes voltage scaling and time borrowing for pipelined circuits, and demonstrated a sizeable reduction in the *energy-delay product* (EDP) and *power-delay product*. Dillen in [16] designed and implemented area-efficient SEFF-based x86-64 AMD microprocessor module and demonstrated enhancements of energy efficiency. In this work, we focus on designing SEFF-based pipelined circuits in the NT regime.

2.2. Soft-edge flip-flop-based pipelines

Fig. 1 illustrates general synchronous SEFF-based linear pipelined circuits. Considering the data consistency between the SEFF-based pipelined circuits and the input and output environments, we impose hard boundary conditions using conventional hard-edge flip-flops at the first and last stage of pipelined circuits. Between the two hard edges, pipelined circuits have multiple combinational logic stages whose delays are affected by process-induced variations. We build stage registers using SEFFs. The key idea is to postpone the clock signal for the master latch, as shown

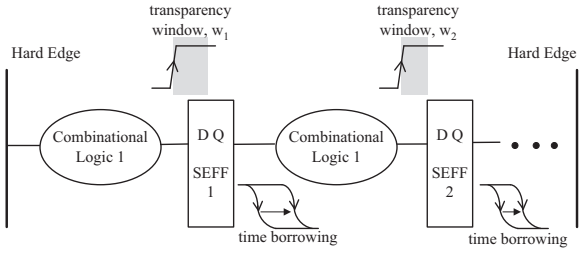

Fig. 1. A linear pipeline with soft-edge flip-flops.

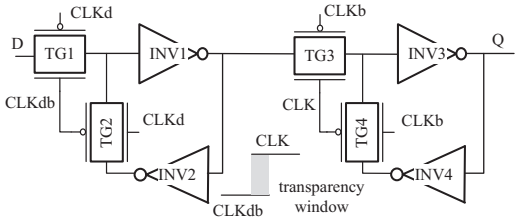

Fig. 2. Design of the positive-edge triggered soft-edge master slave flip-flops.