INTEGRATION, the VLSI journal 43 (2010) 279–288

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

Logical effort based dynamic power estimation and optimization of static CMOS circuits

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ARTICLE INFO

Article history:
Received 19 August 2009
Received in revised form
15 February 2010
Accepted 15 February 2010

Keywords:
CMOS gate modeling
Logical effort
Dynamic power dissipation
Switching power
Optimization
Supply voltage scaling
Transistor sizing

ABSTRACT

This paper introduces a simple and yet accurate closed-form expression to estimate the switching power dissipation of static CMOS gates. The developed model depends on normalizing a gate switching power to that of the unit standard inverter and it accounts for the effect of internodal capacitances. For different loads, gates, sizes and processes, the developed model shows a good agreement with Hspice simulations using BSIM3v3 and BSIM4 models for UMC 0.13 μm and Predictive high-*k* 45 nm processes, respectively. The average error introduced by the model for the considered scenarios is about 3.1%. Depending on the normalized switching power model, two power optimization techniques have been proposed in this paper. The first deals with transistor sizing problem and presents a scheme to size transistors according to a specific design goal. The second technique relies on the joint transistor sizing and supply voltage scaling for reducing the switching power dissipation under specific delay requirements. This technique exhibits superiority over the first for the considered technology processes: UMC 0.13 μm and the Predictive high-*k* 45 nm.

1. Introduction

Power dissipation became a major challenge in Integrated Circuit (IC) design for both high-performance and portable applications. In the high-performance and high-density chips such as microprocessors, high power dissipation limits the number of on-chip transistors and increases the required heat removal, which tends to lower the performance and increase the system cost, size and weight. On the other hand, high power dissipation in battery-operated portable devices such as laptops and cellular phones reduces the battery operation duration and life time as well as increases the battery size and weight. This is important especially with the projected slower improvement in the battery-technology compared to the progress pace of the semiconductor industry [1]. Thus, power estimation, analysis and optimization are essential for CMOS IC design. Using circuit simulators such as Spice to predict the power dissipation in large circuits is an unfeasible solution due to large computing-time. Hence, developing accurate power models is necessary for designing and optimizing very large scale integrated (VLSI) CMOS circuits.

In CMOS circuits there are two sources for power dissipation: static and dynamic. Static power dissipation is mainly due to standby leakage current [2,3] and it is not a function to the switching frequency of a CMOS gate. This source is out of the scope of this work. Dynamic power, in contrast, is the power consumed by a CMOS gate when its output toggles between high and low logic levels [4,5]. Short-circuit power and switching power are the main components of the dynamic power dissipation. The first component is produced by the direct DC path between the supply voltage and ground when both the nMOS and pMOS transistors are ON during the input transition. Switching power, on the contrary, contributes the major portion of the power consumption in CMOS circuits, and is the result of the charging and discharging of the output capacitance.

Reducing the power dissipation in IC designs was always a key concern and the force behind moving from one technology to another. Under specific delay constraints, power may be reduced at different levels of the design abstractions. At the circuit level, which is the target of this paper, power optimization is achieved by transistor sizing, supply voltage and/or threshold voltage scaling.

The works in [6–9] attempt to optimize switching power through transistor sizing. Turgis et al. [6] consider a chain of inverters where a tapering ratio of 4.25 is found to minimize the power dissipation. In [7] it has been proven that the sum of the input capacitances of an inverter chain is minimized when inverters bear the same fanout. For a path with general gates the minimal energy solution was obtained in [8] by numerically solving a set of equations, which was resulted from LaGrange

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doi:10.1016/j.vlsi.2010.02.002

method. BiCMOS circuits were considered in [9]. This method uses an iterative process to size and optimize the design's gates where the high drive capability buffered gates (i.e., BiCMOS) with sufficiently low fan-out are identified and replaced with a lower power unbuffered (i.e., CMOS) version. This work seeks the minimization of network delay subject to network power dissipation.

Optimizing the supply voltage to reduce the power dissipation was the target of many researchers. Considering microprocessors, Cai et al. [10] propose a dual supply voltage technique to reduce both the static and the dynamic power dissipation of CMOS circuits. Low supply voltage and low threshold-voltage devices are used for high activity circuits while higher supply voltage and high threshold voltage devices are assigned to the low activity circuitry. In [11] the power optimization has been achieved in two steps. First, maximum delay is assigned to all gates then in the next step each individual gate is optimized iteratively for minimum power by finding the proper combination of the transistor widths; as well as threshold and supply voltages.

While the trend is to reduce the threshold voltage to reduce the dynamic power dissipation, it has been suggested in [12] that increasing the threshold voltage from $0.2V_{DD}$ (V_{DD} is the supply voltage) to about $0.4V_{DD}$ reduces the total power dissipation significantly at a small cost of delay when it is applied on a chain of inverters.

In [13] a sensitivity-based optimization technique has been developed to tune transistor sizes, the supply voltage and the threshold voltage to minimize the energy in CMOS circuits.

Nevertheless, having low and high voltage supplies causes excessive leakage power whenever low voltage gates directly drive high voltage gates due to the inability of the high outputs of low voltage gates to completely turn off the pMOS transistors of the high voltage gates. This necessitates the use of level shifters (converters) [14], which impose power, delay, area and routing overheads. The impact of these drawbacks can be reduced by clustering same voltage-operated logic together. These clusters can be recognized according to various criteria. In high performance applications, the clusters are formed according to the functionality, and according to the standby power in battery-operated designs [15]. Moreover, clusters could be sorted corresponding to the circuit complexity as macrograin and fine grain islands [16]. At the physical level, the impact of using multiple supply voltages on circuit layout can be reduced by considering well-organized circuit layout, and by developing efficient wiring scheme [17].

Another way of having multiple supply voltages is to dynamically scale V_{DD} to an appropriate level whenever it is possible to cut energy consumption [18]. The optimum value of V_{DD} to achieve minimum power-delay-product is given as a function to the ratio of the widths of the nMOS and pMOS transistors and their threshold voltages [19].

Although modeling the capacitance charging and discharging is well known and published in many text books [20,21], in this paper we use the logical effort philosophy to estimate switching power dissipation as normalized to that of the standard inverter. The developed model is simple, has good accuracy and provides a metric for evaluating the performance of a technology process. More importantly, the developed model is used for power dissipation optimization by determining the optimal transistor sizes. The problem of finding optimal sizes is solved at two levels: the logic-path and gate-transistor levels. At the logic-path level, the relative driving strengths of the gates of a logical path in comparison to each other are determined. For the gate-transistor level, the absolute transistor sizes of each gate of the logic path are calculated to minimize the power dissipation for a target performance. Moreover, the minimum value of the supply voltage is computed by considering the inverter as the representative of the CMOS design, which has been made possible by the normalized power modeling developed in this paper.

Table 1
The definitions of the variable used in the paper.

Variable	Definition
α_v, α_g	The activity factor of an inverter and a gate
α_{nm}	The normalized activity factor
B, b_i	The path and gate branching efforts
C_L, C_{in}	The load and the input capacitances of a path
C_{Lg}, C_{ing}	The gate load and input capacitances, respectively
C_i	The capacitance of a node i that has an electrical path to the gate's output before the switching
C_{ivq}	The input capacitance of the gate's equivalent inverter, which has the same driving-strength of the gate
C_i, C_j, C_k, C_x, C_y	The interondal capacitances at nodes i, j, k, x and y, respectively
C_{out}	The output capacitance of a gate
C_{pg}	The gate parasitic capacitance
C_{tg}, C_{tp}	The input and parasitic capacitance of the template gate, respectively
C_{tn}	The sum of the internodal capacitances
C_{tot}, C_{on}	The total and the on path capacitances of a gate
C_v	The input capacitance of the unit inverter
δ	D_{PDPmin}/D_{LEmin}
d	The normalized delay of a gate
D	The path minimum possible delay
D_α	The normalized delay of a CMOS gate in α fragment
D_{LEmin}	The minimum normalized delay of the logic path
D_{max}	The user delay budget
D_p	The actual minimum path delay (abnormalized)
D_{PDPmin}	The path delay where *PDP* reaches its minimum value
D_{pL}	The value of D_p at V_{DDL}
$\hat{f}$	The optimum gate effort
F and f	The path and the gate efforts, respectively
f_{clk}	The clock frequency
G and g	The path and gate logical efforts, respectively
g_{eff}, p_{eff}	The values of g and p as given by the logical effort technique
g_i, h_i, p_i, b_i	The g, h, p and b of the ith gate respectively
η	A constant that describes the change of a gate input capacitance due to the change of gate size as compared to its template
H, h	The path and gate electrical effort, respectively
κ, λ	Process dependent parameters
N	The number of stages in a path
P	The gate parasitic delay or parasitic power dissipation
P	The logical path parasitic delay
p_n	The gate parasitic switching power dissipation including the intermodal capacitances
P_{nm}	The normalized switching power of a gate
P_{sw}	The switching power dissipation of a gate
P_{swL}	The switching power dissipation of a gate at V_{DDL}
P_v	The switching power dissipation of the unit inverter
p_{vL}	The value of p_v at V_{DDL}
τ, τ_L	The unit inverter delay at V_{DD} and V_{DDL} respectively
t_d	The delay of a gate
V_{DD}, V_{DDL}	The nominal and reduced supply voltage, respectively
V_{tn}, V_{tp}	The threshold voltages of the nMOS and pMOS transistors
W_g, W_{tp}	The widths of a gate and its template, respectively
W_{min}	The minimum width
χ	The voltage-delay proportion constant
Z	A constant describing the ratio of C_{ing}/C_{tg} and C_{pg}/C_{tp}

Table 1 shows the variables used in this paper and their definitions.

The rest of this paper is organized as follows. Section 2 briefly introduces the original logical effort technique. In Section 3, a closed-form expression is developed to estimate the normalized switching power dissipation. This expression is validated in Section 4. Switching power optimization is presented in Section 5 and the paper is concluded in Section 6.