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Towards generic charge-pump phase-locked loop, jitter estimation techniques using indirect on chip methods

Martin John Burbidge[a,b,*], J. Tijou[c]

[a]Faculty of Science and Technology, Lancaster University, Lancs, UK
[b]Institute of System Level Integration, Alba Centre, Alba Campus, Livingston, Scotland, UK
[c]Philips Semiconductors, Millbrook Ind Est, Southampton, Hampshire, UK

Abstract

Due to desirable operational and implementation characteristics, charge-pump phase locked loop (CP-PLL) systems are the architecture of choice for a variety of embedded frequency synthesis applications. A key performance metric of these systems is the spectral purity of the output signal. Spectral purity is difficult to measure directly, especially within a production test environment. This situation is not likely to improve as on-chip system frequencies increase. This paper focuses on specific aspects of a new framework including techniques and methodologies that can detect significant block level errors that lead to spectral degradation. The final crux of the work is to focus towards measurement techniques that can be mapped directly to spectral degradation, and thus prove unambiguously that the CP-PLL system is 'right by design' and free from errors without resorting to difficult direct measurements. This paper provides an overview of typical non-idealities and the associated effects on spectral degradation and also provides explanations of suitable detection methods. It is expected that with ever increasing system frequencies, thorough analysis of the relationship between system non-idealities and jitter/phase noise may be the only option available for rapid production testing of fully embedded CP-PLLs.

Keywords: PLL; CP-PLL; Jitter; Spectral; Degradation; Deterministic jitter; Phase noise; BIST; Partial BIST; DfT

1. Introduction

The key enabling methodology for generation of highly accurate, stable and frequency agile signals for system on chip (SoC) clock generation and radio frequency (RF) synthesis applications is based upon mature phase locking theory. Phase locking theory and application circuits rely on feedback and error control loops that compare a reference frequency with a locally generated signal and provide internal compensation to minimise the phase error between the two signals. Due to desirable characteristics relating to system integration, frequency tracking, and frequency synthesis capabilities, the charge-pump phase locked loop (CP-PLL) is currently the architecture of choice for virtually all SoC and chip-set frequency synthesis requirements. Key design, characterisation and test parameters relating to CP-PLLs consist of loop bandwidth, loop gain, step response and spectral purity of the output signal. These parameters are interrelated. For example, the spectral purity of the output signal within a certain bandwidth is largely defined by the other parameters. Spectral purity is synonymous with phase noise or jitter immunity of the output signal and is often stated as the key system design goal. (Note in following sections, spectral purity, jitter and phase noise will be used interchangeably.) Unfortunately, at very high frequencies with jitter measurement resolution requirements approaching the sub-picosecond range, it can be difficult to assess the performance of the system in these terms. This is particularly true in a production test environment where device insertion board (DIB) connections [1–3], interconnects, and even the die/package pin interface can conspire to corrupt the measurement. In a characterisation environment, it may be possible to resolve some interface problems by careful design of high-speed input/output (I/O) buffers. However, this luxury is not generally

*Corresponding author. Faculty of Science and Technology, Lancaster University, Lancs, UK. Tel.: +44 1524 592983.
E-mail address: m.burbidge@lancaster.ac.uk (M.J. Burbidge).

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available at production test time or when the CP-PLL is resident in the target system [4].

For an ''ideal'' CP-PLL, parameters such as loop gain and loop bandwidth can provide a theoretical and quite accurate approximation to the expected spectral noise performance of the CP-PLL. For instance, within the loop bandwidth, low frequency tracking noise is dominant, whereas outside this range oscillator noise becomes predominant. Generally, by accepting the theory, and carefully designing the CP-PLL blocks using common noise rejection techniques such as, differential oscillators and supply decoupling [5–8], yields jitter/phase noise performance that is beyond the measurement capabilities of contemporary production test systems. This ''right by design'' approach seems to be commonly accepted. Many of the traditional performance metrics can be measured relatively easily in typical characterisation environments using direct access techniques. Typical examples are phase transfer (jitter transfer) function tests and step response tests. Direct jitter or phase noise measurements are also carried out using special purpose instrumentation. Unfortunately, in many cases, due to issues relating to test time and test set-up, the tests cannot be easily transferred to a production test environment. Often, to allow extraction of measurement information during production test, ad hoc design for test (DfT) decomposition methods are used in conjunction with a functional frequency lock test (FLT). The FLT simply checks if the CP-PLL can produce a signal of the correct output frequency within a predetermined time. Typical decomposition methods involve direct measurement of charge-pump currents, and direct stimulation and measurement of the voltage-controlled oscillator (VCO). The results are then compared against pre-defined test limits. The main problem with this approach is that even simple ad hoc direct access test methods can cause problems relating to test access and possible degradation of the CP-PLL output signal [4]. The problems become particularly relevant when addressing the issue of multiple embedded on-chip PLL's.

In the attempt of addressing problems, in recent years there have been various interesting proposals relating to built in self test (BIST) and partial BIST and DfT techniques for CP-PLLs [9–14]. The tests basically focus upon extracting some key parameters using digital only methods. In addition, the method proposed in [10] includes direct jitter measurement circuitry that relies on gate delays for its minimum resolution. Other on chip jitter measurement techniques have been proposed [15–18]. However, these either have measurement accuracy that is limited by gate delays, or require relatively complex analogue tuning techniques to achieve adequate accuracy. The latter case is not particularly applicable to large volume products and retrograde fitting to existing designs. Furthermore, it is questionable if the direct jitter measurements can be tailored to meet the trend towards higher clock frequencies.

This paper generally focuses towards techniques and ideas for investigation of spectral degradation using intelligent decomposition of the CP-PLL in conjunction with well-constructed indirect measurement procedures. The hypothesis is towards identifying how jitter or phase noise manifests itself on the CP-PLL output due to a non-ideality in a particular CP-PLL sub-block. Methods are then proposed that can identify the particular block level non-ideality without having to resort to a direct measurement. Results and ideas are referenced and extended from work relating to a CP-PLL test infrastructure based upon non-invasive digital only ''Ramp Based'' test techniques [7,19]. These papers primarily focussed upon loop gain testing and error detection for key PLL performance degraders, such as forward path leakage. In addition, interesting relationships were observed between loop filter leakage and corresponding spectral degradation. It must be mentioned that although other key papers measured parameters that could have been mapped back to jitter, the relationship was not recognised and subsequent analysis and targeting of the test approaches was not followed through. Furthermore, after the critical relationship between forward path errors and jitter was identified, the decision was made to specifically tailor the ''Ramp Based'' techniques towards spectral degradation estimation. Results of forward path error and jitter correlation based upon the initial observations taken from [19,20] are given in this paper. These papers also provide a more detailed insight into the proposed measurement processes.

This paper consists of the following sections: Section 2, provides a brief description of typical generic CP-PLL operation and identifies the key CP-PLL building blocks. Also, the advantage of employing a generic approach is justified. In addition, typical block level errors, sensitivity in individual building blocks, their effect on the block level performance, relationship to spectral degradation, and possible indirect detection methods are considered. This section also suggests an alternative method for VCO verification. Section 3, outlines structural and functional tests for CP-PLL's based upon ''Ramp Based'' tests. Initial comparisons between forward path leakage and CP-PLL output jitter are also provided. Section 4, provides details of model development for estimation of forward path errors. Section 5, extends the work of Section 3 and attempts to investigate the phase noise spectrum of the PLL output and formally relate this to forward path dispersion measurements. Section 6 briefly summarises the specific advantages of the alternative evaluation techniques. Finally, Section 7 provides suggestions towards further work and additionally provides a summary of the paper.

2. Key CP-PLL block description and block errors related to spectral noise

The purpose of this section is to provide an overview of CP-PLL operation and specifically relate operational blocks to typical errors that can cause spectral degradation at the CP-PLL output. The discussion is focussed towards