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Hot-carrier degradation model for nanoscale ultra-thin body ultra-thin box SOI MOSFETs suitable for circuit simulators

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ABSTRACT

A detailed study of the hot-carrier degradation in nano-scale fully depleted ultra-thin body and buried oxide n-MOSFETs is presented. The degradation mechanisms were identified based on static current–voltage measurements. The degradation of the transistor was explained by considering generation of traps at the gate dielectric/Si interface and traps located within a tunneling distance of the interface. All stress parameters are considered describing with semi-empirical relations their impact on the transistor parameters. Based on our analytical compact model, we propose an aging hot-carrier model predicting with good accuracy the device degradation stressed under different bias conditions using a unique set of model parameters.

1. Introduction

Ultra-thin body and box (UTBB) fully depleted silicon-on-insulator (FD-SOI) MOSFETs have attracted much attention in future sub-28 nm CMOS generations due to their high immunity to short channel effects (SCEs) [1–3]. Furthermore, due to the strong back-to-front gate coupling effect, the threshold voltage of UTBB FD-SOI MOSFETs can be controlled with back gate bias instead of using different channel doping concentrations, thus avoiding variability due to random dopant fluctuations [4]. However, at very small channel dimensions, the electric fields are high implying hot-carrier (HC) degradation issues. Therefore, figuring out the degradation mechanism due to HC is a very important topic in short channel FD-SOI devices.

HC studies in UTBB FD-SOI MOSFETs are limited to few works referred on investigation of the degradation mechanism [5–7] and HC degradation modeling limited in the saturation region [8]. In this paper, we investigate systematically the HC-induced degradation mechanism in short channel FD-SOI MOSFETs by static current–voltage characteristics measurements. Based on our analytical compact model for nanoscale FD-SOI MOSFETs [9], HC degradation model is developed using the threshold voltage shift, the ideality factor shift and the mobility degradation with stress time, predicting the device performance under different bias conditions.

2. Experiments

The HC experiments were performed on FD-SOI n-MOSFETs with channel width W = 0.5 μm and channel length L ranging from 30 to 100 nm, fabricated by STM, France. The front gate stack consists of TiN/HfSiON dielectric with equivalent oxide thickness 1.55 nm, the BOX thickness is 25 nm and the silicon film thickness is 7 nm.

In the HC experiments, the devices were stressed at room temperature by applying stress voltage to the drain and gate electrodes, with the source terminal grounded and back gate bias $V_{bg} = 0$ V. In short-channel devices, it has been confirmed that the worst HC stress condition occurs at $V_{stress} = V_{ds} = V_{gs}$ [10]. The stress was interrupted at selected stress times to measure the front gate transfer characteristics with $V_{bg} = 0$ V, using an Agilent B1500/1530 Semiconductor Device Analyzer. From analysis of the transfer characteristics in the linear region, the degradation of the threshold voltage V_t and the subthreshold ideality factor η were obtained. The threshold voltage was extracted from the transconductance linear extrapolation method [11].

3. Hot-carrier degradation mechanism

Fig. 1 shows typical transfer characteristics of fresh short channel device (L = 30 nm) stressed at $V_{stress} = 1.5$ V for different stress times. Degradation of the threshold voltage V_t, the subthreshold swing coefficient η and the on-state current is observed. The positive V_t shift indicates the built-up of a negative charge in the gate dielectric. The negative charge can result either from electron trapping in the gate dielectric or from generation of acceptor-type interface traps.

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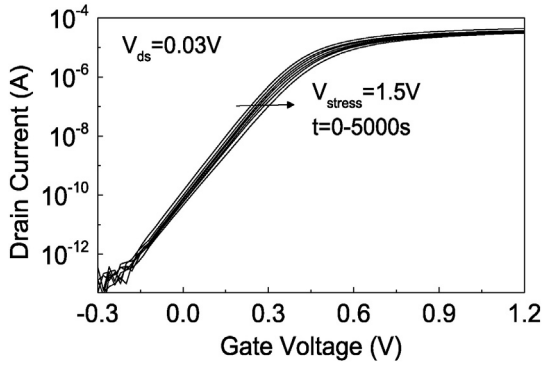

Fig. 1. Transfer characteristics of UTBB FD-SOI MOSFETs with W = 0.5 μm, L = 30 nm stressed at V_{stress} = 1.5 V for different times.

The transfer characteristics before stress, after stress at V_{stress} = 1.5 V for 5000 s and the recovery behavior (after 5000 s at V_{ds} = V_{gs} = 0) are presented in Fig. 2(a). No recovery is observed, indicating that interface and/or bulk trap generation are the main degradation mechanisms, which result in degradation of the transistor parameters.

Fig. 2(b) illustrates the transfer characteristics in the saturation region (V_{ds} = 1 V) before stress and after stress at V_{stress} = 1.5 V for 5000 s in the forward and reverse mode (with the source and drain electrodes exchanged). The drain current is reduced after stress, indicating that the interface trap generation is extended beyond the pinch-off region, as generated hot-carriers dominate over the entire channel length in short-channel devices [12]. In addition, the drain current is further reduced in the reverse mode, indicating that the trap generation is enhanced near the drain region. These findings are supported with the experimental results of a modified charge-pumping technique [13], demonstrating the generation of HC stress-induced interface traps along the channel length and border traps within a tunneling distance

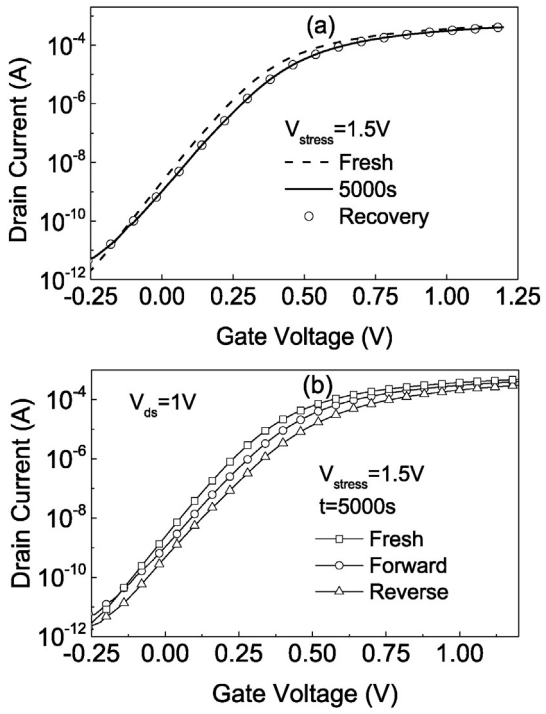

Fig. 2. (a) Transfer characteristics of UTBB FD-SOI MOSFET with W = 0.5 μm, L = 30 nm before stress, after stress at V_{stress} = 1.5 V for 5000 s and a recovery after stress, measured at V_{ds} = 1 V. (b) Transfer characteristics before stress and after stress at V_{stress} = 1.5 V for 5000 s in the forward and reverse modes, measured at V_{ds} = 1 V.

of the gate oxide/Si interface, located above the pinch-off region near the drain.

Fig. 3 presents the threshold voltage shift ΔV_t as a function of stress time of UTBB FD-SOI MOSFETs with channel length L = 30 nm, stressed at V_{stress} = 1.3, 1.5, 1.8 and 2 V. For stress times above 1 s, the positive V_t shift follows a single time dependent power-law of the form $\Delta V_t \sim t^n$ with the exponent n ≈ 0.28, indicating the generation of interface traps [6]. Note that in FD-SOI MOSFETs, the value of n is smaller than that of bulk n-MOSFETs (n ~ 0.4–0.5) for the interface trap generation mechanism and only the front gate interface is degraded during HC stress as shown by a new technique based on capacitance measurements [6]. At short stress times (<0.1 s), it has been demonstrated by fast measurements that the HC degradation is equivalent to the positive bias temperature instability (PBTI) degradation due to the impact of "cold carriers", exhibiting a value for n lower than 0.25 [6].

4. Hot-carrier degradation model

Recently, we developed a complete analytical charge-based compact model for the drain current of nano-scale UTBB FD-SOI MOSFETs, valid in all regions of operation with back gate control [9]. The model includes the device parameters V_t, η and the effective mobility μ_{eff}, which were modeled taking into account the effects of the drain-induced barrier lowering (DIBL), channel-length modulation (CLM), saturation velocity, mobility degradation, quantum confinement, velocity overshoot and self-heating. Thus, modeling the degradation of these parameters could lead to the prediction of the HC-induced device degradation. Analytical models for the threshold voltage with localized interface charges were developed in single-gate bulk MOSFETs [14] and symmetrical double-gate MOSFETs [15]. Because such model is missing for UTBB FD-SOI MOSFETs including localized interface and bulk charges, we provide semi-empirical aging models for the transistor parameters, which are widely used in circuit reliability investigations [16].

The impact on the threshold voltage shift of the stress voltages $V_{stress} = V_{ds} = V_{gs}$ and V_{gs} varying from 1.2 to 2 V with drain voltage fixed at V_{ds} = 2 V is shown in Fig. 4(a) and (b), respectively. The results confirm that the worst case bias condition is at $V_{stress} = V_{ds} = V_{gs}$ following the dependences of the form $\%\Delta V_t \sim \exp(c_1 V_{ds})$ and $\%\Delta V_t \sim \exp[-c_2(V_{ds} - V_{gs})]$. The plots $\%\Delta V_t$ versus $\exp(c_1 \times V_{ds}) \times t^n$ for different values of $V_{stress} = V_{ds} = V_{gs}$ demonstrate that all the data points lie on a straight line for n = 0.277 and $c_1 = 3.64\ V^{-1}$ (Fig. 5a) and the plots $\%\Delta V_t$ versus $\exp[-c_2(V_{ds} - V_{gt})] \times t^n$ for different values of V_{gs} with fixed V_{ds} = 2 V demonstrate that all the data points lie on a straight line for n = 0.277 and $c_2 = 1.2\ V^{-1}$ (Fig. 5b). Fig. 5(c) presents the dependence of the $\%\Delta V_t$ with the reciprocal of the channel length, induced by HC stress at V_{stress} = 1.8 V for different stress times. The inset of Fig. 5(c) presents the relationship between the $\%\Delta V_t$ degradation and 1/L, showing that the V_t degradation is strongly dependent on the channel length. For the UTBB FD-SOI devices of the present

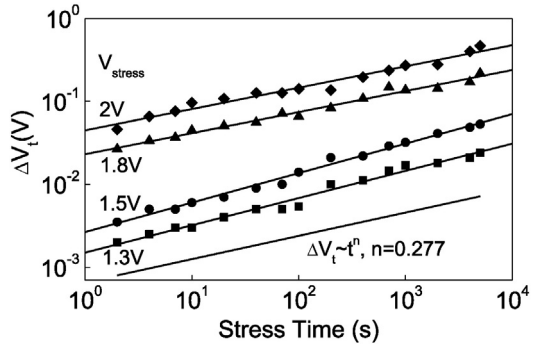

Fig. 3. Threshold voltage shift ΔV_t with stress time under different stress bias V_{stress} conditions.