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# Top-down fabrication optimisation of ZnO nanowire-FET by sidewall smoothing

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ABSTRACT

This paper describes the optimisation of top-down fabrication process of the ZnO-based dual nanowire field effect transistors (NWFETs) based on the spacer method. The approach uses the top-down nanowire process with reduced sidewall roughness during pattern transfer to improve the electrical characteristics. The main feature of the process involves a reflow of the photoresist performed at a temperature of 130 °C and dry oxidation of the etched silicon sidewalls. The process optimisation leads to a significant reduction of the root-mean-square (rms) roughness of the photoresist from 23.2 nm to 3.6 nm and the ZnO nanowire rms surface roughness from 11.2 nm to 5.5 nm. The ZnO-based NWFET fabricated with the resist reflow process operates in depletion mode with a threshold voltage of −6 V, a subthreshold slope of 0.80 V/decade, an on–off current ratio of $10^6$, a transconductance of 5.9 nS and field effect mobility of 7.7 $cm^2$/Vs.



## 1. Introduction

One-dimensional (1D) semiconductor nanostructures such as nanowires, nanotubes, nanorods and nanoribbons have attracted intensive research effort due to their unique electrical and optical properties [1]. Among these nanostructures, nanowires are preferable because they demonstrated promising potential application in transparent electronics, optoelectronics, sensors, and solar cells [2,3]. In particular, ZnO nanowires are attractive due to their wide, direct band gap (Eg ~ 3.37 eV at 300 K), large exciton binding energy of 60 meV and low material cost [3].

There have been many reports published on ZnO nanowire field effect transistors (NWFETs) fabricated either by bottom-up or top-down process. Bottom-up process can be based on vapour–solid, solution–phase and vapour–liquid–solid method, where the nanowire is synthesized from the assembly of adatoms [4]. Top-down fabrication of nanowire consists mainly of deposition and anisotropic etching of the material on planar substrate [5]. Hence, it can provide nanowires in well-defined locations on a wafer and permits nanowires with various lengths to be fabricated on the same chip. Although bottom-up process can achieve high crystallinity, good morphology and large aspect ratio of nanowires, the process often randomly aligns the nanowires on the device substrate and does not produce uniform nanowire dimensions [6–8]. Moreover, it is difficult to address nanowire FETs into position with bottom-up process.

Top-down fabrication method could resolve the number of challenges associated with bottom-up method by control of size and location of the NWFETs. Previous studies of top-down ZnO nanowire field effect transistors (NWFETs) showed significant variation of electrical characteristics, such as output drain current and field effect mobility [9,10]. One of the possible causes is the nanowire surface roughness from fabrication process, which can induce trap charges density and influence the device characteristics [11]. Based on theoretical investigation done by [12–14], surface roughness is shown to have significant effects in nanowire electrical properties. In top-down fabrication process, the possible source of surface roughness is during pattern transfer in photolithography and etching process [15]. Roughness introduced during photolithography originated from different causes, including mask quality, photoresist performance and image projection transfer [16].

In this study, we focus on optimising the top-down spacer method with reduced sidewall roughness originating from the photoresist edge roughness and to improve the electrical characteristics. We fabricated ZnO devices from our non-reflow resist with $SiO_2$ pillar spacer method [9,10] and reflow resist with oxidised silicon trenches spacer method. Both fabrication methods use standard photolithography, remote plasma atomic layer deposition and anisotropic dry etch. The thermal reflow process which is inspired by the work described in [17], can reduce the sidewall roughness of the patterned photoresist. Further roughness reduction can be achieved by thermal oxidation of the etched silicon sidewall and provide an improved ZnO and gate oxide interface [18]. The electrical characteristics of the ZnO NWFETs from the non-reflow and reflow resist process were then compared to give an insight of the effect of surface roughness.

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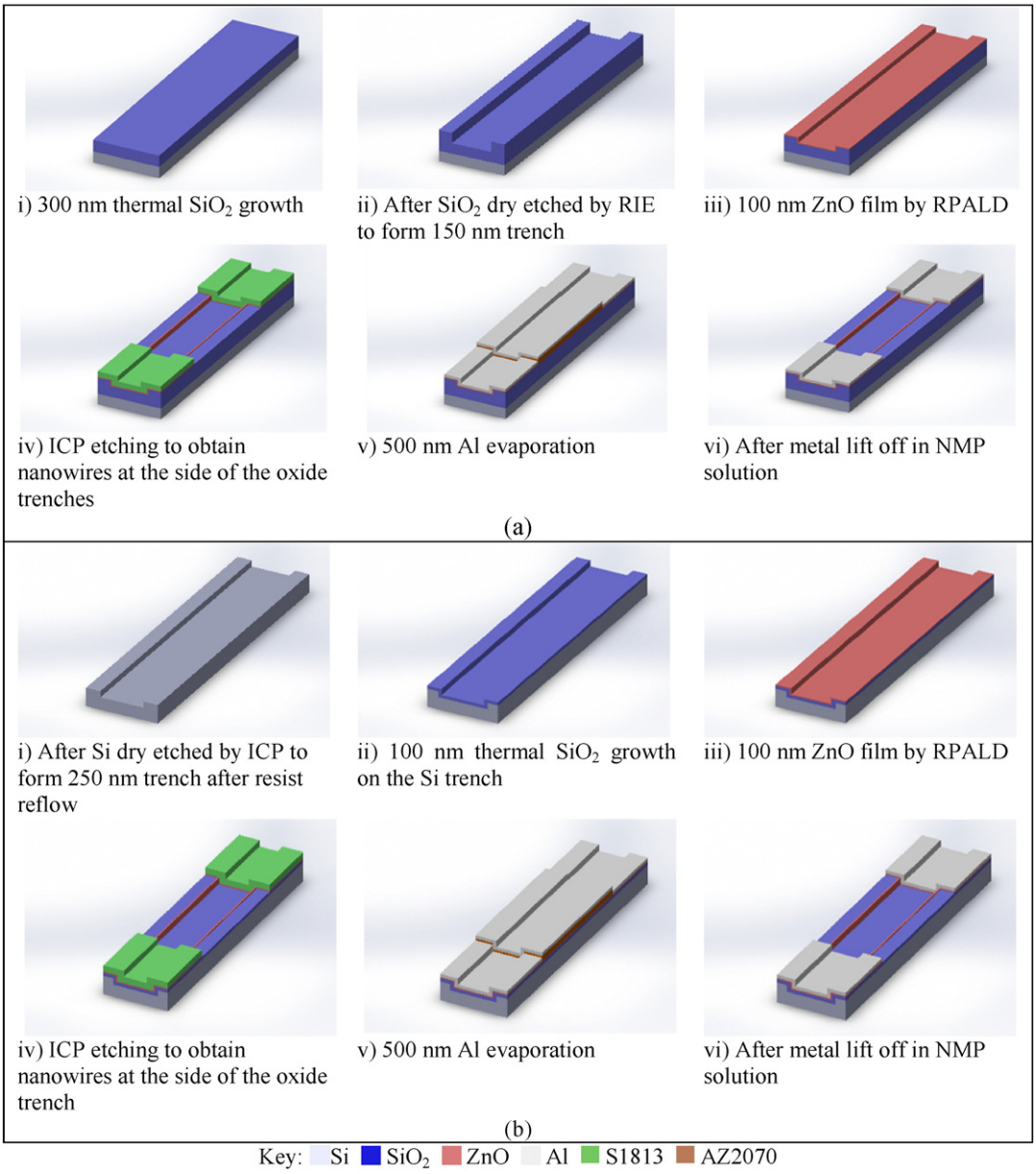


**Fig. 1.** Schematic of the fabrication process for (a) non-reflow resist spacer method and (b) reflow resist spacer method.

## 2. Experiment

We fabricated both of ZnO NWFETs based on non-reflow resist and reflow resist spacer method. A detailed description of top-down fabrication based on non-reflow resist spacer method has been reported in our previous work [9,10]. The non-reflow resist process starts with a p-type Si sample and a layer of 300 nm $SiO_2$ thermally grown on the substrate. The $SiO_2$ was then etched anisotropically by reactive ion

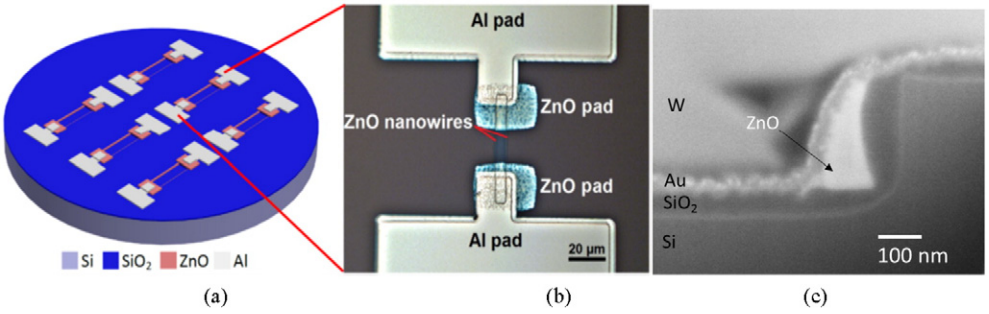


**Fig. 2.** (a) Schematic drawing of the processed NWFET array, (b) optical microscope image of dual nanowires and (c) scanning electron micrograph of the trench section of the fabricated NWFETs (Au = gold coating, W = tungsten coating for focused ion beam cross-sectioning).