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ZnO nanoparticle thin-film transistors on flexible substrate using spray-coating technique

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ABSTRACT

Nowadays, transparent and flexible electronics allow the fabrication of several innovative products, from flexible displays to radio-frequency identification tags and wearable electronics. For this reason, this technology has gained the interest of several companies including the scientific community. In flexible microelectronic systems, thin-film transistors (TFTs) are the active elements switching the driving currents. Therefore, we present inverted coplanar ZnO nanoparticle TFTs on a freestanding polyethylene terephthalate (PET) substrate. For the active semiconductor deposition a spray-coating technique was used availing the process to large area substrates. The maximum process temperature was limited to 115 °C. Subsequently to the integration process, the electrical and optical characteristics of the transistors were evaluated.

1. Introduction

During the past few decades, flexible and transparent electronics are being actively researched by several companies and by the scientific community [1,2]. With this technology, the fabrication of a wide range of innovative products will be possible, from flexible displays to radio-frequency identification tags and wearable electronics. Along with this, the possibility to integrate devices on large area substrates at low-cost using high throughput processes are the main reasons for this interest. Thin-film transistors (TFTs) are essential for this technology, as they are used as active elements providing the driving currents in the future systems.

In order to integrate devices on flexible substrates, the materials and the integration processes have to be carefully selected to be compatible with the used substrate. For example, the maximum process temperature and the influence of the chemicals used during the device fabrication, as solvents, acids and alkaline solutions, have to be considered matching the substrate requirements [3]. On the one hand, polymeric substrates commonly present adequate optical characteristics (transmittance in the visible light spectrum), which extend the possible commercial applications. On the other hand, these substrates show low temperature resistance and chemical stability, as well as lack of dimensional stability (substrate shrinks at high temperature), which increases the misalignment between different films and electrodes. Another crucial material in the integration process is the chosen active semiconductor. Nowadays, new materials, as DNTT or C_8-BTBT, which present the possibility to be deposited using solution methods, may improve the integration process and the electrical characteristics [2,4]. Metal oxide semiconductors also play an important role in this technology. Different materials and compounds, as IZO, ZnO, GIZO, IGO and ZTO, have been studied [1]. Due to the outstanding electrical and chemical properties, ZnO is a key semiconductor. Additionally, ZnO is transparent in the visible light spectrum (ZnO energy bandgap = 3.4 eV [5]), which makes it a good candidate for the fabrication of transparent and flexible devices. As vacuum techniques, e.g. sputtering, are not entirely suitable for the low-cost market, the use of nanoparticle dispersions is a good approach to fabricate cost-efficient devices on large areas and flexible substrates.

Moreover, to simplify the integration process on flexible substrates, shadow masks are commonly used. Applying this method no photolithography and etching steps are required, avoiding the chemical contact to the substrate and previously deposited layers. Controversially, the use of shadow masks limits the structure resolution to around 10 μm or larger, depending on the deposition method and mask density. Further issues related to the layer reliability and the mask fixing system are faced when large area substrates are used. To avoid the mechanical stress suffered by the template during the integration process, the substrate is commonly fixed to a rigid mechanical support, e.g. a Si wafer. However, this technique does not make use of the substrate flexibility and masks possible defects originated from the mechanical stress during the device processing. Conjointly, a damage-free release of the flexible substrate is complicated and requires extra processing steps increasing the production cost. Therefore, the devices are generally electrically characterized without removing it from the rigid mechanical support. In case of a

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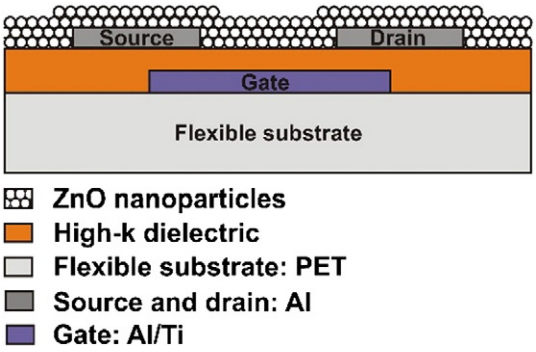

Fig. 1. Schematic cross section of the ZnO nanoparticle TFT on a flexible substrate.

transfer to an integration process without this support, this can lead to an unexpected variation of the transistor electrical characteristics.

2. Integration process

In this study, we avoid the use of a rigid mechanical support and present an integration process of ZnO nanoparticle TFTs on a freestanding 75-μm thick polyethylene terephthalate (PET) substrate. Furthermore, the reported integration routine can be adapted to be used with organic semiconductors. The schematic cross section of an inverted coplanar TFT is depicted in Fig. 1. Since the PET foil is not attached to a rigid substrate, the foil is allowed to bend during the integration process. Nevertheless, during the dielectric deposition and photolithography processes, the substrate is shortly fixed by a vacuum system. This fixing system enables a more realistic scenario reproducing the mechanical stress endured by the substrate on a later large-scale production using, for example, roll-to-roll technique.

For the gate electrodes, a stack of 50 nm aluminum and 7 nm titanium was evaporated under high vacuum conditions and structured by conventional photolithography and wet etching techniques. As gate dielectric, a high-k nanocomposite ($k = 12$ [6]) based on hydrolyzed and partial condensed ethyl silicates filled with TiO_2 was used. This organic–inorganic nanocomposite combines the advantages of the polymeric matrix (e.g. flexibility) and of the inorganic compound (e.g. high dielectric constant). The spin-on gate dielectric was cured at a temperature of 115 °C followed by an UV irradiation step. Via connections were opened through the gate dielectric using photolithography and wet etching processes to contact the gate electrodes. For the drain and source electrodes, a 150-nm thick aluminum was evaporated under high vacuum conditions and defined by photolithography and wet etching techniques.

The next step consists of the deposition of the active semiconducting layer. Here, depending on the properties of the semiconductor and deposition methods, the characteristics of the gate dielectric surface play an important role in the deposition quality. For example, if a water-based solution is used, the hydrophilic surface achieved by the etching process will lead to a formation of a reliable layer. Controversially, the drain and source electrodes can be structured by a lift-off technique, which leads to a hydrophobic surface. For inorganic semiconductors deposited by vacuum techniques, as sputtered ZnO, the surface properties of the gate dielectric will not directly influence the deposition quality. Nevertheless, the surface energy may induce a shift on the electrical characteristics of the transistors or, in the case of organic semiconductors, a different crystalline growth.

Subsequently to the template fabrication, a water-based ZnO nanoparticle dispersion (Nanophase Technologies Corporation) was sprayed onto the templates and annealed at 115 °C in a convection oven under ambient conditions. Fig. 2 depicts a scanning electron microscope image of the nanoparticulated layer using a Jeol JSM-6300F. It is possible to observe a uniform deposition of the nanoparticles and their predominantly spherical shape, as well as an average particle size of about 70 nm, which is also in agreement with the nanoparticle datasheet [7]. In order to stabilize the semiconducting layer, an UV irradiation step combined with a high relative humidity treatment was performed [8]. Fig. 3 depicts an optical microscope image showing an integrated set of TFTs, as well as an image of the flexible substrate.

Another important aspect of our process is the resolution of the photolithography technique on the PET substrate. The process quality was analyzed using an Olympus LEXT 3D Measuring Laser Microscope OLS4000. Fig. 4 depicts an image from the photolithographic step with a resolution of about 1 μm for the definition of the drain and source electrodes prior to the etching of the aluminum layer. As a consequence of the temporary vacuum fixing system, it is possible to align different masks sustaining the definition of multiple layers on a freestanding flexible substrate.

Additionally to the resolution achieved in the lithography, the material of drain and source can be interchanged. This flexibility in the template fabrication avails the same process to different semiconductors. The choice of the material to a specific semiconductor will depend on the position of the work function of the material with respect to the valence/conduction band of the inorganic semiconductor or the frontier molecular orbitals (highest occupied molecular orbital, HOMO, and the lowest unoccupied molecular orbital, LUMO) if an organic semiconductor is used. For example the use of gold for the drain and source electrodes enables the evaluation of organic semiconductors as pentacene or DNTT [2]. Nevertheless, the use of other materials for the electrodes (source, drain and gate) and interconnections will also

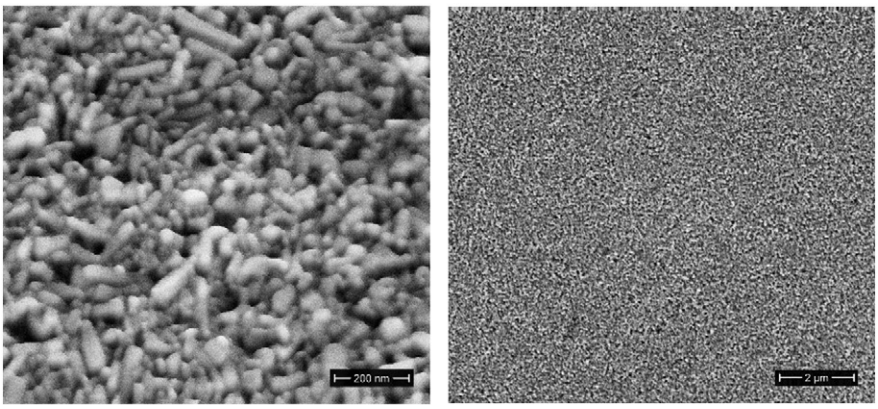

Fig. 2. Scanning electron microscope images of the ZnO nanoparticulated layer.