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A depth analysis for different structures of organic thin film transistors: Modeling of performance limiting issues

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ABSTRACT

This research paper is focused on finding reasons for performance diversity between top contact (TC) and bottom contact (BC) structures of organic thin film transistors (OTFTs). The electrical characteristics, device physics, performance parameters and conduction mechanism are deeply analyzed using Atlas–Silvaco numerical device simulator. The simulation methodology consists of different approaches based on mapping of crucial issues for OTFTs. Few calibration are common for both TC and BC structures like material parameters along with Poole–Frenkel mobility model, defects in bulk OSC, dipoles at OSC–dielectric interface, correction for drain offset current and elimination of contacts voltage drop. After mapping of these issues, the results for TC structure are found close to the reported experimental results. However, performance of BC structure is reasonably matched only after incorporating some additional fabrication based issues such as unfilled corners and low mobility region around the S/D contacts. The drive current and the mobility are obtained higher by four and three times, respectively for TC than that of BC structure. Also, the sub-threshold slope is improved by 50%. On the contrary, the threshold voltage is lower by 8% for BC structure due to closer proximity of contacts to the dielectric interface.

1. Introduction

A gradual and noteworthy advancement on the organic electronics front has been endowed with an alternative design platform, especially in the application areas of flexible analog and digital circuits. Over the last two decades, significant research and development has been done for the organic material based devices, motivated by the need of large area display circuits complying with low-end applications. A novel class of thin film transistor comprising of organic or polymeric semiconductor consents to implement the electronic functionality on the paper [1], plastic foil [2] and fiber [3] substrates that too at a very low cost. Some leading applications of organic TFTs include solar cell [4], sensors [5], e-paper [1], static random access memory [6], organic light emitting diode [7] and flexible integrated circuits [8].

An OTFT exhibits a thin film of OSC, an insulator and three electrodes; source (S), drain (D) and gate (G). It is realized in a layered structural design, wherein, S/D electrodes make direct contact with semiconductor while gate remains isolated through the insulator. [9]. Several researchers including Luo et al. [10], Waldrop et al. [11], Warta et al. [12] and Assadi et al. [13] reported organic TFTs on the glass and flexible substrates and now these transistors are at the verge of commercialization. The performance of OTFT depends on the several factors such as; structural dimensions of different layers, trap states, work function difference of adjacent layers, carrier injection, charge per unit area and interface barrier [14]. Additionally, the position of S/D electrodes with respect to the OSC–dielectric interface plays an important role in determining the performance. It is owing to dissimilar path traversed by the charge carriers from source to drain electrode [15] for different structures. Two dimensional bottom gate structures with contacts in top and bottom; bottom gate top contact (BGTC/TC) and bottom gate bottom contact (BGBC/BC), are shown in Fig. 1(a) and (b), respectively.

Several researchers have reported higher performance [16–19] for the top contact due to higher charge carrier injection area and low contact resistance. Despite of low performance, BC structures are promising for cost-effective flexible electronic applications, since, they can be fabricated through simple printing techniques that makes them highly suitable for large area display applications [20]. In this work, various empirical parameters are incorporated to model the behavior of top and bottom contact OTFTs. The electrical characteristics and performance parameters are analyzed after mapping of each possible limitation associated with these transistors.

This paper is arranged in five sections, including the current introductory Section 1. Thereafter, Section 2 describes the simulation setup used to analyze the performance of TC and BC OTFTs, which includes device dimensions, mobility model and materials along with their

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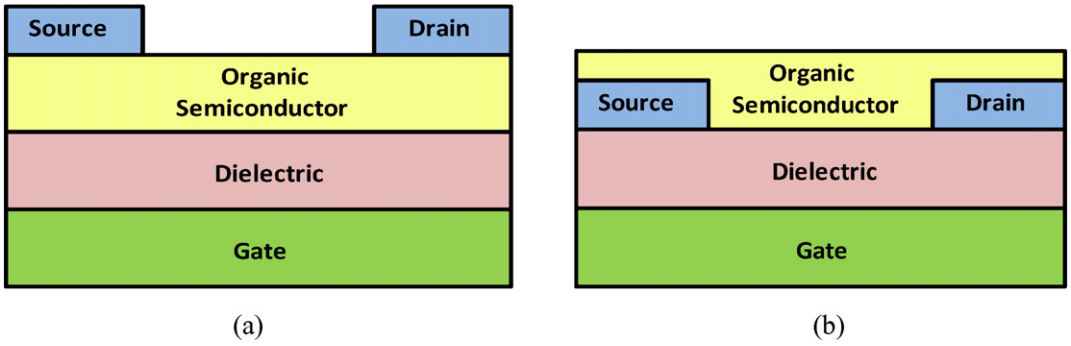

Fig. 1. Bottom gate OTFT schematics with (a) Top and (b) Bottom contact OTFT structures.

properties. Furthermore, Section 3 incorporates common issues related to both transistors along with their mapping to model the actual behavior. Some additional simulation strategies are introduced in Section 4 to incorporate some fabrication based issues in the BC structure, as well. Finally, Section 5 summarizes important outcomes of the proposed work.

2. Simulation setup

To observe the characteristic differences between top and bottom contact OTFTs, these structures are analyzed using benchmarked industry standard organic module of Silvaco Atlas 2-D numerical device simulator [21]. This simulator has been proven useful in comprehending the device physics in detail. Moreover, it allows the users to incorporate their own defined materials. Fig. 2(a) and (b) illustrate the simulated structures highlighting current flow lines for top and bottom contact structures, respectively.

Different layer's materials, typical structural dimensions and material parameters are summarized in Table 1. Additionally it includes model parameters such as zero field activation energy, hole Pool–Frenkel factor and doping concentration, N_A. Undoubtedly, the external doping is meant for inorganic semiconductors only. Here, the N_A term is used in the simulation to enable the original concentration of holes in the pentacene semiconductor, as per the requirement of used simulator. This concentration is calculated by the relation as [24]:

$$N_A = \frac{V_T \ C_I}{q \ t_{OSC}} \tag{1}$$

where V_T, q, t_{OSC} and C_I symbolizes for threshold voltage, carrier charge, thickness of organic semiconducting layer and gate dielectric capacitance per unit area, respectively. The capacitance of both TC and BC organic transistors is calculated as 1.475 nF/cm^2 with relative dielectric constant of 3.0 for the PET, dielectric material.

In the simulation process, individual regions are formed in a mesh that comprises of complex grid of triangles, where the model entails the calculations [21]. Therefore, a high degree of accuracy can be achieved by assigning a high density of meshing grids as shown in Figs. 3 and 4. Besides this, it exhibits finite element based algorithm that incorporates a high degree of convergence in the device and circuit implementation. To predict the results under proper boundary conditions, Poole–Frenkel mobility model is applied, which is expressed as [19,21]

$$\mu(E) = \mu_0 \exp\ \left[-\frac{\Delta}{kT} + \left(\frac{\beta}{kT} - \gamma\right)\sqrt{E}\right] \tag{2}$$

where $\mu(E)$, μ_0, E, k and T correspond to the field dependent mobility, zero field mobility, electric field, Boltzmann constant and temperature, respectively. Additionally, parameters Δ and β represent the zero field activation energy and hole Pool–Frenkel factor, respectively, whereas; γ is used as a fitting parameter. This model demonstrates the conduction due to field enhanced thermal excitation of trapped charge carriers. As the gate voltage increases, mobility also improves and thus justifies the hopping transport phenomenon in OTFTs.

3. Performance of top and bottom contact OTFTs

The electrical characteristics and parameters of both structures are analyzed with the same dimensions, materials and operating conditions to make an appropriate comparison between them. The performance is observed in terms of driving current capability (I_D), mobility (μ), threshold voltage (V_T), sub-threshold slope (SS) and current on–off ratio (I_{ON}/I_{OFF}) in the subsequent sections.

3.1. Incorporating materials and model parameters

Primarily, the electrical characteristics and performance parameters of TC and BC transistors are analyzed by considering materials and model parameters summarized in Table 1. The drain characteristics of top and bottom contact structures, as a function of gate voltage are illustrated in Fig. 5(a) and (b), respectively. Top contact structure exhibits higher current in comparison to bottom contact even with same structural dimensions and materials. This justifies performance dependency on the layered structural design due to formation of channel with regards to the S/D contacts [15]. The drain current, I_D is obtained as 96 and 72 μA at $V_{DS} = V_{GS} = -100$ V for top and bottom contact OTFTs, respectively. The performance of organic transistors strongly depends on the charge carrier injection area. The top contact current is higher due to comparatively a larger injection area for the charge carriers than that of bottom contact, leading to a lower contact resistance [25] and thereby a higher current.

In top contact structure, the carrier injection/extraction depends on the electrode length (horizontal edge), however, in bottom contact, the carrier's inject from the vertical edge of source. This is the main reason for performance dependence of BC transistors on the S/D electrode thickness [19]. For the justification of the carrier injection, the hole concentration is analyzed horizontally (S to D) across the device length. Resulting curves are illustrated in Fig. 6(a) and (b) for TC and BC structures, respectively.

In TC structure, this concentration is highest across the source length. On the contrary, this concentration across S/D electrode length is nil in the BC structure but sufficient holes are available in the channel. Besides this, the holes are incremented in the channel with respect to increasing V_{GS} for both structures. Furthermore, the hole concentration is also observed at the vertical edge of the source (near channel) and a combined plot for both structures is illustrated in Fig. 7. Now, the holes are not available in the TC across the vertical edges of the contacts, whereas, they are present in the BC structure. This shows that the charge carrier injects/extracts from the horizontal edge of the source/drain in TC but from the vertical edge in BC transistor. Since, the length of source and drain electrodes is higher (10 μm) in comparison to the height (40 nm), therefore, the carriers injection is more in the top