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Electrical properties of self-aligned gate-all-around polycrystalline silicon nanowires field-effect transistors

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ABSTRACT

Low temperature (≤600 °C) polycrystalline silicon nanowires field-effect transistors have been developed following a top-down approach and classical photolithography techniques. N channel transistors have been tested with a single top-gate, bottom-gate and gate-all-around architecture in order to compare their electrical performances in relation to the interface state density. Analysis shows that surrounding gate enables control of parameters such as on-current, subthreshold slope and threshold voltage and offer potential further applications.

1. Introduction

As integrating smaller sized high performance electronic devices have become a key point over the past decades, innovative transistor designs have emerged. Chip-to-wafer density has to remain high to be competitive so size reduction is still a burning issue and non-planar devices are part of these brand new products. As a consequence, multigate field-effect transistors (FET) have been developed [1]. Dual-gate (DG) [2], tri-gate [3], FinFET [4] and gate-all-around (GAA) FET [5–7] are the main structures, based on various materials, described in literature and available on the market. In such new gate architecture passing from 2D to 3D, silicon nanowires (SiNWs) FETs seem to be one of the most attractive choices. They enable to avoid problems due to short channel effect such as threshold voltage (V_{TH}) "roll-off" [8] or drain induced barrier lowering (DIBL) [9]. More precisely, surrounding-gate transistors where the gate circles the nanowire channel allow a better electrostatic gate control. SiNWs can be prepared by a bottom-up method like layer by layer self-assembly [10], vapor–liquid–solid growth techniques [11], plasma-enhanced chemical vapor deposition (PECVD) [12] or using matrix template [13]. Nevertheless, the silicon nanowire growth process for device integration remains difficult as their size and positioning cannot always be perfectly controlled. In addition, SiNWs need to be selectively collected and handled in a planar layout. Most recent methods such as roll-to-roll technique enable SiNWs printing in order to obtain desired shapes and structures [14].

Top-down approach favors patterning architectures in a planar layout, most of the SiNWs are patterned on silicon-on-insulator (SOI) substrates by etching the first silicon layer down to buried oxide [15] because it provides best electrical performances for SiNW based FETs but the main drawback remains the high cost of these substrates. Several nano patterning techniques such as e-beam [16], atomic force microscopy [17] or deep-UV [18] were developed to achieve SiNWs. These high cost fabrication methods are not compatible with mass production. However, polycrystalline silicon SiNWs (poly-SiNWs) synthesis using sidewall spacer top-down method [19–21] seems to be a lower cost alternative, fully compatible with planar complementary metal oxide semiconductor (CMOS) silicon technology.

Moreover, SiNWs FETs have nowadays attracted a lot of attention for the development of mechanical [22], biological [23] or chemical [24] sensors. In the latter two cases, SiNWs are used as sensitive units to detect charged chemical species, responsible for variation of the channel conductance. In particular, top-gate and back-gate transistors based on poly-SiNWs made by the spacer method showed to be good candidates to gas (ammonia) detection [25], pH sensing [26] and DNA hybridization [27].

GAA FETs are mainly known for enabling full channel depletion [6] so as to improve subthreshold slope (SS) and having low threshold voltage for identical subthreshold leakage current [28]. In addition, using double-gate devices proved interesting in relation to circuit drift compensation [29] because it allows dynamically fixing the threshold voltage as the second gate is able to control electrostatic effects (*e.g.* drift problems in organic light emitting diode (OLED) displays [30] or sensors [31]).

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In this paper, we develop a low temperature (≤600 °C) fabrication process of top-gate, bottom-gate and GAA FETs. SiNWs are made using the spacer method which is an original technique for GAA transistors fabrication. Independent biasing of each gate allows a possible threshold voltage control of these bottom-gate transistor (BGT) and top-gate transistor (TGT). In addition, electrical connection of both bottom and top-gate electrodes allows the formation of a gate that surrounds the channel, creating GAA architecture. Electrical performances are analyzed as a function of the density of state highlighting oxide/semiconducting nanowire interfaces difference in top and bottom-gate configurations.

2. Experimental details

Poly-SiNWs FETs are fabricated using a 4 masks and a CMOS compatible fabrication process. N-type transistors with parallel poly-SiNWs channels are fabricated using the sidewall spacer method described below, where the spacer at nano scale made of poly-Si constitutes the nanowire. The key nanowire fabrication steps are illustrated in Fig. 1 (not to scale). Substrate is firstly covered with a 1.2 μm thick silicon dioxide (SiO_2) insulating layer deposited by Atmospheric Pressure Chemical Vapor Deposition (APCVD) technique at 420 °C (not shown). Then, a 750 nm thick highly N-type *in-situ* doped amorphous silicon

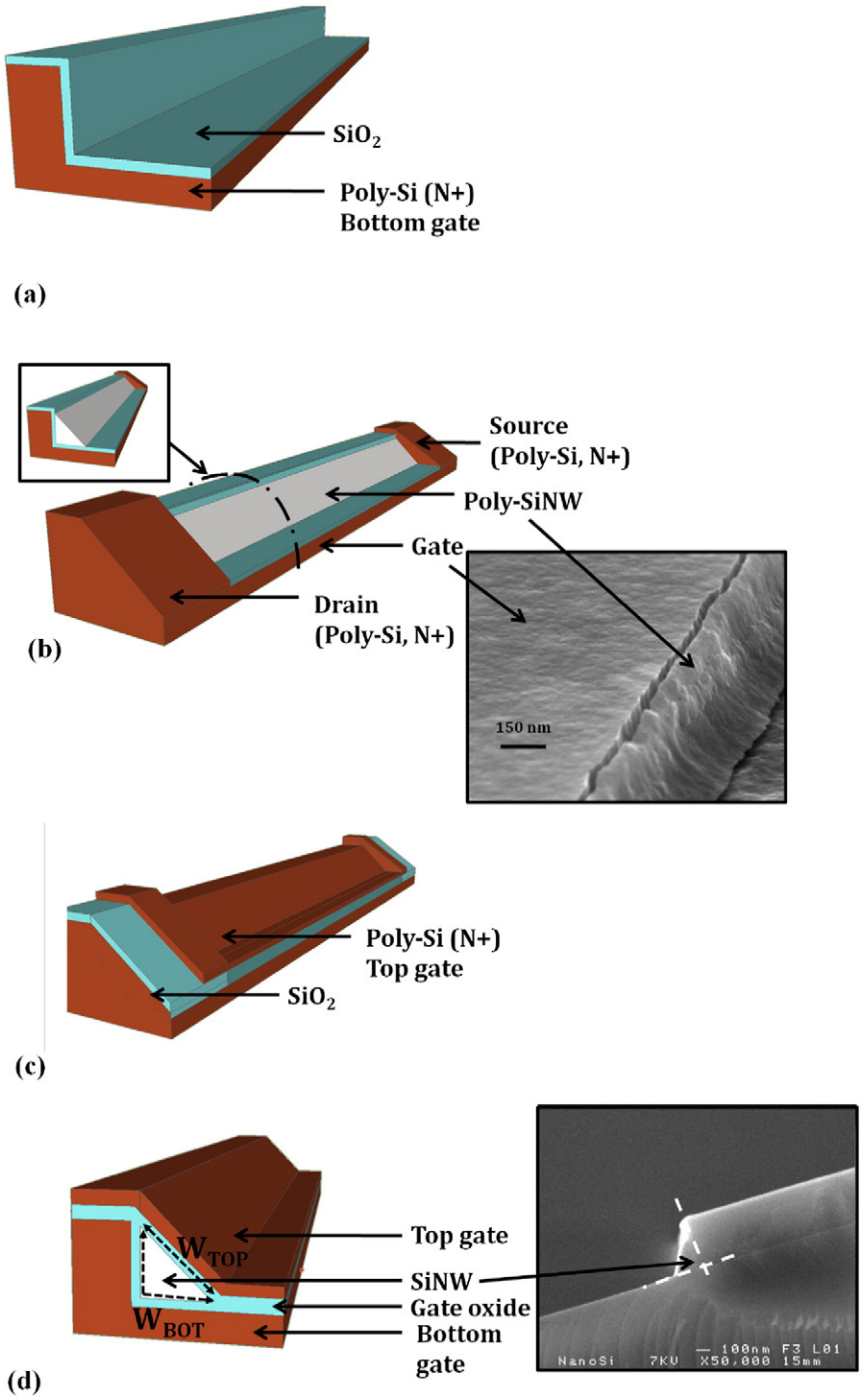

Fig. 1. Gate-all-around field-effect transistor fabrication steps: (a) stepped bottom-gate patterning and bottom oxide layer deposition, (b) polycrystalline silicon nanowire channel and drain-source zone formation and SEM image, (c) top-gate formation and (d) cross section of the final device with main dimensions : L = 5 μm, W_{TOP} = 420 nm, W_{BOT} = 600 nm per nanowire and SEM cross-section view of a silicon nanowire.