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Ambient-atmosphere annealing effect on the carrier conduction behavior based on the linear-regime transfer characteristics of pentacene thin film transistors

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ABSTRACT

The linear-regime transfer properties of the annealed pentacene-based organic thin film transistors (OTFTs) in air at various temperatures up to 375 K are examined. It is found that the linear-regime carrier mobility increases with increasing annealing temperature reaching a maximum at 350 K, and then decreases with further increasing of annealing temperature beyond that point. However, an increase in annealing temperature leads to the shift of the threshold voltage towards positive gate-source voltages. An analysis through the temperature-dependent transfer characteristics of OTFTs reveals that the increased carrier mobility is the result of the reduced values of the hopping distance and the barrier height for hopping.

1. Introduction

Organic thin film transistors (OTFTs) were extensively studied for applying to organic light-emitting diode panels, active-matrix flat panel displays and flexible logic circuits, due to their mechanical flexibility and low-cost process [1]. In particular, pentacene is an organic semiconductor, which attracts the interests of scientists and engineers and it has been used as an active channel layer of OTFTs [2–13]. The performance of the pentacene-based OTFT is mainly determined by its carrier mobility, which is influenced by the electron–phonon coupling, crystallinity and intermolecular bonding nature [2–4]. Charge transport in organic semiconductors has been extensively studied [14–21]. The thermal annealing effect on carrier transport for the pentacene transistor was investigated [5–9]. Although considerable effort has focused on explaining annealing-influenced variations in the OTFT properties in terms of the pentacene film morphology, the crystalline polymorph, and the electronic transport and the traps induced at the pentacene/gate dielectric interface, the effect of annealing treatment on the temperature-dependent charge movement in the pentacene transistor has received less attention. This study focused on the thermal annealing effect of the charge transport characteristics of the pentacene-based OTFT that is exposed to air. The hopping transport in the pentacene transistor is analyzed. It is found that the hopping distance (a_h) and the barrier height for hopping ($q\phi_t$) play important roles in determining the linear-regime filed-effect carrier mobility (μ).

2. Experimental details

Four-inch Si (100) wafers purchased from Woodruff Tech Company were used in the experiment. The resistivity of the heavily doped n-type Si (n^+-Si) wafer is about 0.001 Ω cm. The n^+-Si film thickness was about 525 μm. A SiO_2 layer was grown on the n^+-Si wafer using a dry oxidation process as a gate oxide layer. The thickness of the SiO_2 film, as estimated using an ellipsometer, was 265 nm. The insulator capacitance per unit area (C_i) of 12 nF/cm^2 was obtained from capacitance–voltage measurement. A 70 nm thick pentacene (Luminescence Technology Corp.) layer was deposited on the SiO_2/n^+-Si substrates by vacuum thermal evaporation and the evaporation rate was 1.8 nm/min. The substrate temperature was fixed at 90 °C. Then, the source and drain electrodes were fabricated by depositing Au metal on the pentacene layer through a shadow mask. The devices have the channel width (W) of 700 μm and the channel length (L) of 100 μm. The pentacene-based OTFTs were annealed in air at 325, 350 and 375 K for 1 min on a hotplate, respectively. The surface morphology of the pentacene films was studied using atomic force microscopy (AFM). The linear-regime transfer characteristics of OTFTs were measured using a Keithley Model-4200 semiconductor characterization system. The drain current (I_D) versus gate-source voltage (V_{GS}) curve in the linear region was scanned from 10 to −40 V, with a fixed

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drain-source voltage (V_{DS}) of −2 V. The I_D–V_{GS} characteristics were measured in the temperature range from 300 to 330 K by steps of 10 K. The V_{GS}-dependent I_D measurements for a constant V_{DS} provide a method to examine the relationship between the threshold voltage (V_{TH}) and μ.

3. Results and discussion

Fig. 1 shows the linear-regime transfer characteristics as a function of annealing temperature. By fitting a $|I_D|$–V_{GS} curve based on the equation of $|I_D| = |(0.5\mu WC_i / L)[2V_{DS}(V_{GS} - V_{TH}) - V_{DS}^2]|$, the values of V_{TH} and μ are derived. Table 1 shows μ and V_{TH} of OTFTs without annealing. Table 1 also shows μ and V_{TH} of OTFTs annealed at 325, 350 and 375 K. Fig. 2 shows μ (V_{TH}) as a function of annealing temperature. It is found that μ increases with increasing annealing temperature reaching a maximum at 350 K, and then decreases with further increasing of annealing temperature beyond that point. Ji et al. [9] found that annealing below a certain critical temperature point (70 °C) improves the carrier mobility, but a further increase beyond the critical point (70–160 °C) degrades the carrier transport. In addition, the on/off current ratios (I_{on}/I_{off}) for experimental devices, taken from log(I_D) versus V_{GS} characteristics, are all included in Table 1. It is shown that the derived value of I_{on}/I_{off} increases with increasing annealing temperature reaching a maximum at 350 K, and then decreases with further increasing of annealing temperature beyond that point. It is believed that the most significant factor allowing obtaining higher μ and I_{on}/I_{off} is the improved quality of the pentacene layer [21]. On the other hand, it is found that an increase in annealing temperature leads to the shift of V_{TH} towards positive gate-source voltages. The V_{TH} shift is attributed to the trap charge densities at the pentacene channel/gate oxide interfaces [22]. Moreover, the existence of electron traps near the pentacene/dielectric interface of extrinsic origin was proposed by Völkel et al. [23]. We suggest that thermal annealing changes the interfacial properties of pentacene/SiO_2, inducing the positive shift of V_{TH}.

In order to understand this phenomenon and to determine the possible changes in the carrier transport behavior and the correlation between annealing treatment and performance, an analysis through the temperature-dependent transfer characteristics is presented. Fig. 3 shows the temperature-dependent linear-regime transfer characteristics of OTFTs without annealing. Fig. 4 shows the temperature-dependent linear-regime transfer characteristics of OTFTs annealed at 350 K. The carrier conduction mechanism in the pentacene film has been considered to be hopping dominated [24–27]. To the hopping conduction, the conduction current increases as temperature (T) increases, and this is resulted from thermally excited electrons hopping from one trap state to another trap state in the pentacene layer. In order to discuss and investigate the electrical conduction mechanism, the temperature-dependent $|I_D|$–V_{GS} curves are measured and compared. The inset of Fig. 3 shows the ln($|I_D|$)–(1000/T) curves in the linear region for V_{GS} = −27, −30, −33 and −36 V, respectively. The inset of Fig. 4 shows the ln($|I_D|$)–(1000/T) curves in the linear region for V_{GS} = −27, −30, −33 and −36 V, respectively. The linear ln($|I_D|$)–(1000/T) curve is found, indicating that the hopping conduction is the dominant process. The hopping conduction can be expressed as [28–30]

$$I_D = Sqa_m n_e v_f \left[\exp\left(\frac{qa_m V_a}{2dkT} - \frac{q\phi_t}{kT}\right)\right] \quad (1)$$

where S is the contact area, d is assumed to be the film thickness, q is the elementary charge, V_a is the applied bias, a_m is the mean of hopping distance, n_e is the density of space charge, v_f is the intrinsic vibration frequency, and k is Boltzmann's constant. The slope (S_L) was derived from Arrhenius plots (the inset of Fig. 3 or 4). Then, we fitted the linear curve with a vertical axis of S_L and a lateral axis of V_{GS}. As a_m represents for a_h, the values of $q\phi_t$ and a_h are derived from the fitting linear curve. Fig. 5 shows $q\phi_t$ (a_h) as a function of annealing temperature. This finding confirms that charge transports are affected by annealing which leads to the fluctuation in the values of $q\phi_t$ and a_h.

The above results revealed that $q\phi_t$ and a_h influence on the I_D–V_{GS} characteristics by controlling the hopping conduction, which induces the different temperature-dependent transfer characteristics. Due to the disordered molecular structure of the most organic semiconductors, hopping occurs between localized states [26]. The hopping probability for conduction in organic semiconducting materials depends on the

Table 1
The linear-regime filed-effect carrier mobility, threshold voltage and on/off current ratio of OTFTs.

	μ ($cm^2\ V^{-1}\ s^{-1}$)	V_{TH} (V)	I_{on}/I_{off}
OTFTs without annealing	0.09	−11.1	1×10^5
OTFTs annealed at 325 K	0.13	−5.7	3×10^5
OTFTs annealed at 350 K	0.15	−3.4	1×10^6
OTFTs annealed at 375 K	0.05	7.2	5×10^4

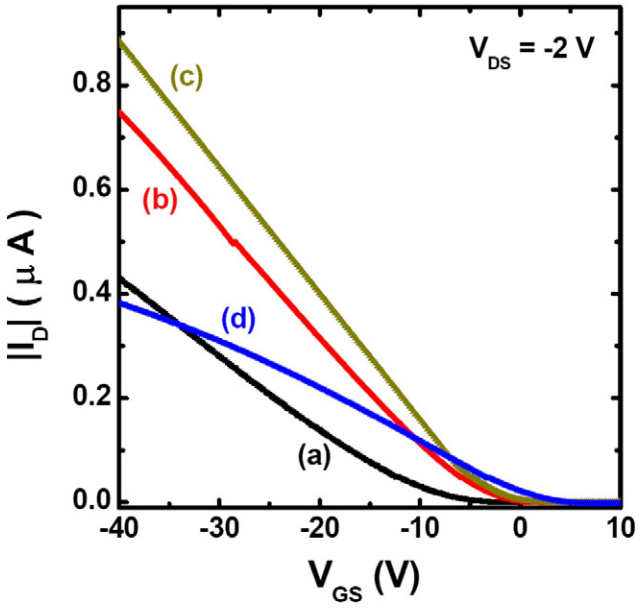

Fig. 1. The linear-regime transfer characteristics as a function of annealing temperature [(a) OTFTs without annealing and OTFTs annealed at (b) 325, (c) 350 and (d) 375 K].

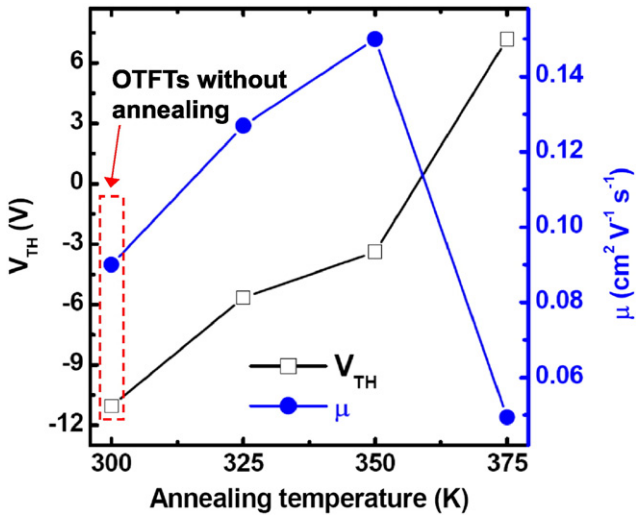

Fig. 2. μ (V_{TH}) as a function of annealing temperature.