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Measurement-based electrical characterization of through silicon vias and transmission lines for 3D integration

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ABSTRACT

Measurement-based electrical characterization of through silicon via (TSV) and redistribution layer (RDL) is of great importance for both fabrication process and system design of 3D integration. This paper presents the electrical measurements and analysis of TSV and double-sided RDL test structures, from DC to high frequency up to 40 GHz. TSV shows great dependence of DC resistance and leakage current on fabrication process. An inverse V-shaped C–V curve is presented between adjacent TSVs in N-type silicon substrate, from −10 V to 10 V. In the high frequency characterization, two methods are proposed and applied to extract resistance and inductance of a single grounded TSV. Individual transmission loss of TSV, RDLs on top and bottom surface of silicon substrate are calculated, and corresponding circuit parameters thereof are extracted to characterize their electrical properties precisely.

1. Introduction

With increasing demands for smaller, multi-functional electronic devices, 3D integration with through silicon via (TSV) has attracted substantial attention and has been already on the way to commercialization. It provides vertical interconnects with high integrated density, greatly reduced interconnect length, low power consumption, heterogeneous integration, high system speed and small form factor [1–4]. Many 3D integration architectures have been proposed to address different applications, including MEMS, CMOS image sensor (CIS), stacked memories, and so on. Nevertheless with these sophisticated 3D integration technique, TSV and redistribution layer (RDL) remain the key components for signal transmission. According to the functionality requirements, a wide range of different signals (digital, analog, RF etc) exist in the electrical system. It is mandatory to thoroughly investigate the electrical behavior of TSV and redistribution layers, both at DC and RF/microwave frequencies.

So far, electrical modeling and simulation of TSV have been done in lots of previous works. Several equivalent circuit models have been proposed for TSV, and analytical expressions of its RLCG parameters were derived. Kim et.al [5] proposed an equivalent circuit model for TSVs arranged in a ground-signal configuration. The values of RLCG parameters were tied to the geometrical and physical parameters of TSV based on two-conductor transmission line theory. Salah et al. [6] used a π-type equivalent circuit model for a single TSV inside grounded silicon substrate, and the dimensional analysis method was used to derive the expressions of RLCG parameters. Liu et al. [7] applied magneto-quasi-static theory and developed a rigorous resistance-inductance model of TSV, considering the skin effect and proximity effect of TSV at high frequency. Impact of physical parameters of TSV on its transmission performance were also widely studied, such as TSV height, diameter, pitch, liner thickness, cross-section shape, substrate resistivity, etc. [8–11]. Fundamental design rules can be drawn based on these parametric analyses. DC resistance, leakage current and C–V measurement of TSV have been widely used for process evaluation in previous works [12–15]. Gu et al. [16] evaluated the loss and crosstalk properties of RDL transmission lines on silicon substrate. A TSV–RDL-bump test vehicle was measured up to 20 GHz in [5], and the measured S parameters agreed well with the ones calculated from the equivalent circuit model. Ndip et al. [17] extracted the inductance and capacitance of GSG–TSV from single-port open and short TSV test vehicles, in the 100 MHz to 40 GHz frequency range. Dual-port TSV chain structures were measured in [18], and RLCG parameters of TSV were extracted based on empirical formulas and 3D full wave electromagnetic simulations. Four-port test vehicle with two grounded TSVs were applied in [19]. Coupling capacitance and conductance were extracted. In the above-mentioned studies, some only dealt with experimental results without sufficient analysis. As measurement analysis is of great concern

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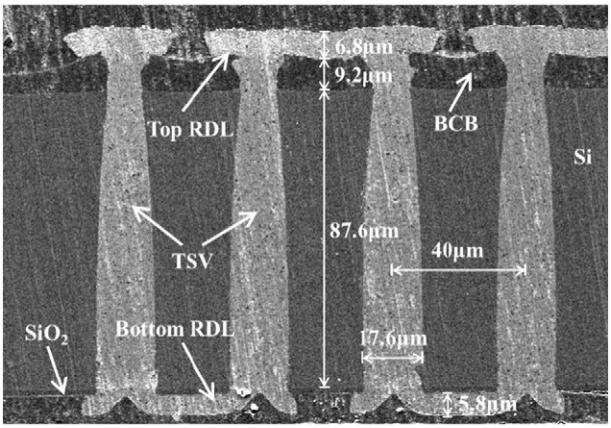

Fig. 1. SEM cross section of the fabricated structures with TSV and metal lines on both sides of the silicon substrate.

to both fabrication process and system design, there is still room for improvements in the studies of measurement-based characterization of TSV and RDL.

In this paper, electrical measurement and analysis of TSV and RDL structures are carried out, from DC to high frequency up to 40 GHz. Test structures are designed and fabricated based on an in-house fabrication process [20–21]. DC resistance, leakage current, and C–V curves are measured to evaluate the basic properties of TSV and RDLs. A test vehicle with a grounded TSV is applied to study the frequency-dependent properties of TSV's resistance and inductance. Accuracy is improved with a new de-embedding method. Another test vehicle with GSG–TSV and RDL transmission lines is measured to show the signal integrity of the interconnect path for 3D integration. The contributions of TSV, RDL transmission line, and test pad to the total transmission loss of the test vehicle are calculated respectively, and RLCG parameters of TSV and RDL transmission line are extracted and analyzed for design recommendations.

2. TSV–RDL structure description

Several test structures are fabricated to analyze the electrical properties of TSV and RDLs, which consist of TSVs and RDLs on both top and bottom surface of silicon substrate. Fig. 1 is the scanning electron microscope (SEM) image of the fabricated TSV and double-sided RDL structures. TSVs are etched with DRIE (deep reactive ion etching) equipment and filled with electroplated copper. The fabricated TSVs show a tapered cross-section, with 17.6 μm in diameter and approximately 99 μm in depth. TSVs are isolated with SiO_2 from Si substrate. The SiO_2 liner is no thicker than 0.5 μm due to the difficulty of high aspect ratio deposition. As shown in Fig. 1, copper RDLs on the top and bottom surface of the silicon substrate are electroplated with a thickness of 6.8 μm and 5.8 μm respectively. RDLs on the top side are lined with a 9.2 μm thick BCB (benzocyclobutene) layer from Si substrate, and bottom RDLs are deposited on a SiO_2 layer, which is less than 2 μm thick. N-type silicon substrate is thinned to 87.6 μm, of which the average bulk resistivity is 3.1 Ω cm by four-point probe measurement.

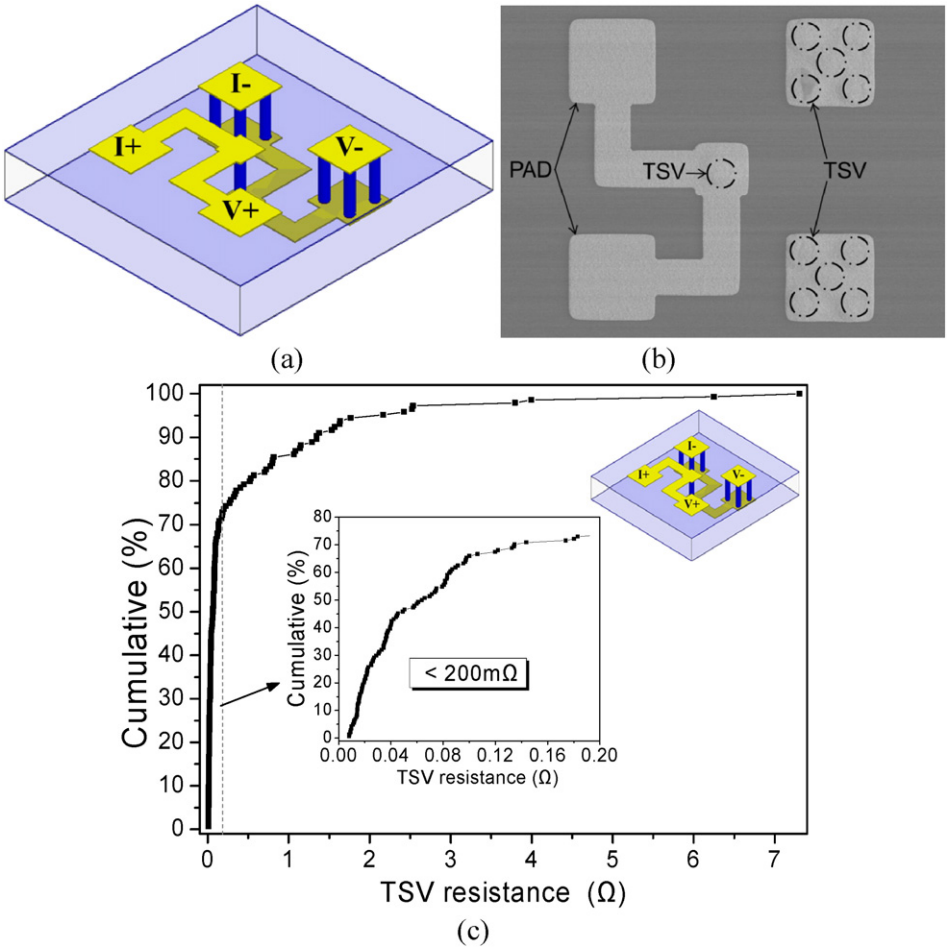

Fig. 2. Four-point Kelvin structure for TSV resistance measurement, (a) 3D model, (b) SEM image in top view, (c) distribution of measured single TSV resistance, the inset shows resistance distribution below 200 mΩ.