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Parallel SER analysis for combinational and sequential standard cell circuits ☆

Weiguang Sheng *, Jianfei Jiang, Zhigang Mao

Department of Micro/Nano Electronics, Shanghai Jiao Tong University, Shanghai 200240, China

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ABSTRACT

A parallel SER (soft error rate) evaluation framework ASSET-VLG was developed to analyze the SER of both combinational and sequential standard cell circuits. ASSET-VLG was constructed in practically oriented way: (i) it employs a verilog parser for automatically reading the synthesized DUT (device under test) netlist; (ii) it provides an accurate and unified SER analysis framework for both the combinational and sequential circuits rather than the former only; (iii) it targets to a 130 nm production library and the modeling method can be easily ported to newer technologies. Furthermore, concurrency is also exploited for accelerating the evaluation procedure on modern multi-core computers. These features make ASSET-VLG appropriate for automatic SER estimation in design stage and can be easily integrated into current highly reliable ICs design flow. Experiments on ISCAS'85 and ISCAS'89 benchmark circuits show the evaluation time ranges from 0.5 ms to 2.16 s without previous memory explosion problem. Compared with spice, the modeling method of ASSET-VLG provides 98% accuracy. The parallelizing experiments indicate the proposed method has better scalability, e.g., 4.44 X speedup are obtained in a 4 cores/8 threads platform. The experiments also reveal that sequential part (flip-flops) in the circuit dominating the system SER by one order than combinational gates for a 130 nm CMOS process. Last but not least, significant frequency dependence of SER are observed in flip-flops, implying the commonly used critical charge measure is insufficient for characterizing soft error in sequential cells.

1. Introduction

Soft error due to high-energy particles striking has been a main challenge for modern deep sub-micron CMOS ICs. The particles include α particle emitted from the radioactive impurities in package materials, and neutron or proton come from high-energy cosmic rays. As technology scaling, even the harmless muon in the past has become a newer soft error source in nanoscale circuits [1].

Soft error seriously affects the reliability of ICs, while robust circuit design requires solutions to the accurate, automatic and systematic SER (soft error rate) estimation methodologies [2]. Soft error rate has various metrics: in logical level, FIT (failure in time, one failure per billion device hours) is used to measure the circuit SER [3]; while for storage elements, cross section or critical charge is used instead [4]. The most straightforward SER estimation method is to use particle accelerator or heavy-ion equipment to bombard the DUT (device under test) [5]. However, the bombarding approach is expensive and only applicable when chip has been fabricated. Designers demand distinctive SER evaluation tools designated for design stage.

In the past decades, intensive researches have been carried out for characterizing circuit SER in design stage to mitigate the gap between circuit design and reliability evaluation [6–11]. These works can help us estimate SER in design stage promptly and avoid the high reengineering cost after taping out for reliability issue. SER evaluation tool has been a key factor for highly reliable circuit design flow.

Though great advancements have been achieved, SER evaluation is still an open research problem, especially in making the methodologies more systematic, automatic, fast and industry-oriented [2]. We developed a new tool ASSET-VLG (Advanced Statistical SER Evaluation Toolkit for Verilog) to address the aforementioned problems. ASSET-VLG contains a bunch of programs developed using C++ and Python language, which reads in DUT's gate level netlist generated by logic synthesizer, and performs SER estimation fully automatically.

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* Corresponding author.
E-mail addresses: wgshenghit@gmail.com (W. Sheng), jiangjianfei@sjtu.edu.cn (J. Jiang), maozhigang@sjtu.edu.cn (Z. Mao).

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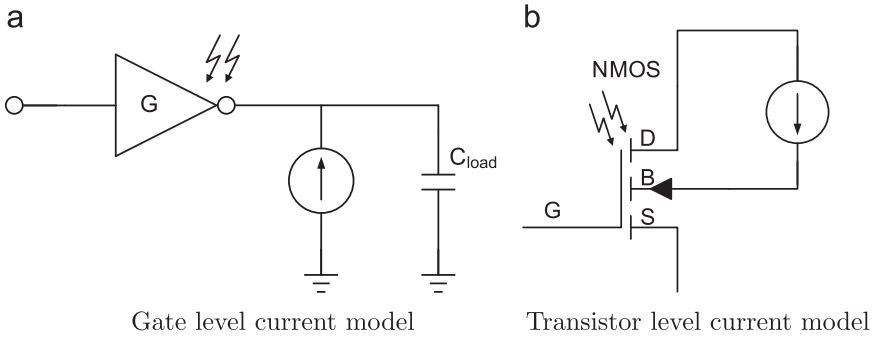

Fig. 1. Current models for SET glitch generation.

The contributions of this paper can be summarized as follows:

1. It provides a systematic methodology to analyze SER of various circuits. Both combinational and sequential logic can be analyzed by ASSET-VLG, while many previous researches are designated for only one specific type circuits.
2. The entire SER evaluation flow of ASSET-VLG is fully automated by various accompanied automation tools: library modeling, input vector preparation, SER analyzer, etc.
3. LUT (lookup table) with trilinear interpolation approach is utilized to model the single event glitch generation and propagation, providing at least 98% modeling accuracy compared to spice simulator.
4. As known to us, it might be the first time multithreaded parallel programming techniques were introduced to the SER analysis realm by utilizing the power of modern multi-core platform. Although [9] had exploited the bit-level parallelism (at the cost of ignoring electrical masking) emerged in the logic simulation field.
5. A fast frequency aware SER analysis tool for flip-flops was developed by combining statistical fault injection and curve fitting techniques. By using this tool, we found there are dramatic frequency dependence of flip-flop SER. The same phenomenon was also investigated by a recent work utilizing a different method and technology [12].
6. With the help of ASSET-VLG, we found that sequential logic (flip-flops) dominating the SER of 130 nm benchmark circuits. Similar results was also obtained by a circuit level SER estimation tool ASSET-SPI developed by us on the 180 nm technology, which reminds us the main soft error challenge before 130 nm technology still comes from the sequential cells rather than the combinational part predicated in other works.

The rest of this paper is organized as follows: Section 2 reviews the backgrounds and related works; Section 3 describes the theoretical framework of ASSET-VLG; Section 4 detailedly describes the implementation of ASSET-VLG and solutions to some key problems; Section 5 gives experimental results and the discussions on the results; Section 6 concludes the whole work.

2. Related works

In circuits, particles striking the reverse biased transistor will generate a small voltage glitch (SET, single event transient) at the drain node. The glitch might be latched by a succeeded storage elements (latch or flip-flop) and destroy its original value, thus a SEU (single event upset) or soft error occurs. As technology scaling and operating frequency increase, SET originating from combinational logic has much more chances to get latched by storage cells and upsetting the chip. It is believed that for the technology beyond 100 nm, SER from combinational logic will exceed the sequential logic and dominate the chip SER [13,4]. However, recent researches in [14,15] show that sequential logic soft errors still dominate at features sizes as small as 32 nm, e.g., for a 32 nm bulk CMOS process, the SER of one single logic chain is less than 10% of the nominal latch SER at 1 GHz [14]. Therefore, both the combinational and sequential logic should be taken into account in the comprehensive SER analysis.

Researches in [16,17] employed Monte Carlo based technique to model soft error from physical perspective with too many lower details, which made the technique time-consuming and applicable for device level modeling rather than higher level large-scale SER analysis. Simulated fault injection technique can also be used to evaluate chip SER by injecting soft error into DUT's simulation model [18,19]. However, fault injection has two disadvantages: (i) it requires large number of injections to obtain statistical unbiased results; (ii) simplified bit-flip model used in fault injection loses the glitch width and amplitude details, which makes it more appropriate for gross SER estimation at the behavioral level.

Analytical SER evaluation methodologies make good trade-off between accuracy and resource requirements. It models the SET glitch generation and propagation by analytical approach to obtain the SER estimation of DUT. Generally spice results are utilized as the golden standard to evaluate the accuracy of analytical methodologies. For SET glitch generation, Fig. 1 shows two SET current models mostly adopted in analytical approaches, where one is for gate level modeling and the other is for more detailed transistor level modeling. In Fig. 1(a), a current source is attached at the gate output to model the SET glitch generation, while in Fig. 1(b) the current source is inserted between the drain and the body of the transistor [20]. The latter is more close to physical reality because any transistor in gate may get struck but Fig. 1(a) assumes only gate output is struck by particles.

Generated SET glitches will propagate in the circuit and may be latched by storage elements. The propagation and latching of SET are affected by three masking mechanisms [13]: (i) logical masking – there must exist a sensitive path from the striking site to the primary output for the SET propagation, otherwise the glitch will be filtered out; (ii) electrical masking – SET without enough amplitude or width will be attenuated by gate in the data path and evaporate eventually; (iii) latching-window masking – SET must reach the flip-flop in legal latching window to be latched successfully. Various methods have been proposed to model the SET glitch generation and propagation to estimate the SER by analytical approach.

ASERTA in [21] used fault simulation and heuristic rules to compute the logical and electrical masking probability to estimate the soft-error tolerance of nanometer combinational circuits. In [22,10], complicated analytical equations were employed to model the SET propagation to storage cells, and then compute the combinational logic SER based on fault simulation. Refs. [23,8,24] used