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An efficient design of full adder in quantum-dot cellular automata (QCA) technology

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ABSTRACT

The full adder circuit is a basic unit in digital arithmetic and logic circuits. In this paper an improved full adder in QCA technology is proposed. This design is considerably declined in terms of cell numbers and area, compared to other full adders and delay is kept at minimum. To design this full adder a different formulation for sum and carry outputs of full adder has been used. The simulation results in QCADesigner software confirm that the presented circuit works well and can be used as a high performance design in QCA technology. Finally, the proposed QCA full adder is used to make three sizes of ripple carry adders (RCA) and acceptable results are achieved.

1. Introduction

In the near future, it is expected that the CMOS technology reaches to the end of its roadmap because of many serious challenges such as short channel effect, impurity variations, high cost of lithography and more importantly, the heat [1–3]. So, many technologies such as Single Electron Transistor (SET), Resonant Tunneling Diode (RTD), Carbon Nanotube Field Effect Transistor (CNFET) and Quantum dot Cellular Automata (QCA) have been emerged to solve the mentioned problems [3–5]. According to the international technology roadmap for semiconductors (ITRS) report which offers an accurate summary of future technologies, QCA is one of the promising future solutions [6].

The QCA is a powerful alternative to use in VLSI circuits because of its ability to achieve high performance in terms of device density, clock frequency and power consumption [4,7,8]. This technology is based on a specific physical phenomenon, called Coulomb repulsion, which uses location of electron pairs instead of voltage levels for logical modes. The data is represented by cells polarizations, which are controlled by inputs and clock signals [7,9]. A key advantage of QCA devices is the simplified interconnection which is possible with this paradigm. Since the cells communicate only with their nearest neighbors, there is no need for long interconnection lines. The inputs are applied to the cells at the edge of the system and the computation proceeds until the output appears at cells at the edge of the QCA array [10].

Physical and algorithmic based designs are two different aspects which are studied in QCA. In high level designs, concentration is on the logical and algorithmic design as well as the physical design. However, physical interactions can be disruptive in device performance. Therefore, control of the physical interactions is a necessary problem in the real QCA circuit designs, especially in large systems [11].

The circuits in QCA technology have been designed and improved in the terms of area, complexity, and delay. Many logical devices such as memory [12,13], adders [5,14–20] and sequential circuits [21–27] are implemented in QCA technology. The fabricatable layout designs of QCA are also proposed in [26–28].

This paper introduces a new QCA full adder design using a different formula for sum which is enhanced in term of cell numbers in comparison to other approaches proposed in the literature. Using this approach provides improved area and delay to other recent designs. For evaluating the proposed QCA full adder in larger adders, we have designed the ripple carry adders (RCA) using the proposed full adder in sizes of 4-bit, 8-bit and 16-bit which have significant features.

This paper is organized as follows. A brief background of QCA architecture is studied in Section 2. We have reviewed previous presented circuits of one-bit full adders and their QCA layouts in Section 3. Section 4 is introduced our proposed one-bit full adder

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circuit and its new formulation for sum is proved. In Section 5, the layout of proposed QCA full adder and the simulation results are described and a comparison has been done between the proposed full adder and some recent implementations for evaluation. Finally, we have concluded this paper in Section 6.

2. Architecture of QCA

In this part, some basic concepts of QCA technology including logic gates, interconnections and clocking are described.

2.1. QCA cell

The QCA cell is a square structure in nano-scale that consists of four quantum dots and two electrons. The electrons are able to tunnel between quantum dots if the potential barrier that separates quantum dots is low. According to Coulomb repulsion, electrons occupy two opposite corners of the cell. Consequently, the four quantum dots in each QCA cell can be in two stable polarization states. These states can be used to encode binary information. Two configurations for the cells can be created by occupation of corner dots as shown in Fig. 1. The −1 and 1 polarizations are equal to binary values zero and one, respectively [9]. In QCA technology, switching is succeeded by switching the occupancy of the two electrons [19].

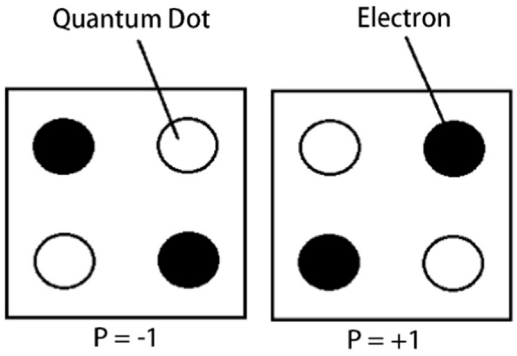

Fig. 1. QCA cell.

2.2. Logic gates

The topology of the QCA layout defines the interaction of the cells and hence the functionality of the overall circuit [19]. All conventional logic gates can be constructed using QCA cells. The majority gate is the basic block of QCA circuits. Fig. 2 (a) demonstrates the structure of the majority gate that consists of three input cells, one inside cell and one output cell.

The tendency of the inside cell is moving to a ground and consequently it gets the polarization of the majority of its neighbors. The inside cell will tend to follow the majority polarization since it represents the lowest energy state [5].

An AND gate or OR gate will be obtained by fixing the polarization of one input to the majority gate as logic 1 or logic 0. As demonstrated in Table 1, if one input is set to 0, the majority gate gives the AND of the two other inputs. Also, if one input is set to 1, the majority gate gives the OR of the two other inputs. We can use the advantage of this property in design of circuits.

The other structure block is the inverter gate which has different layouts in QCA designs. The schematic and different layouts of the inverter gate are shown in Fig. 2(b). According to the Coulomb repulsion, the lowest energy state for two diagonally adjacent cells is when they have opposite polarities.

The QCA designers can implement all logical functions with a combination of majority gates and inverter gates [5].

2.3. QCA circuit internal connections

Input data is carried down arrays of QCA cells due to interaction of adjacent cells. Binary data is transmitted from one physical location to another location by a wire. Once the polarization of a

Table 1
Truth table of majority gate.

A	B	C	M(A, B, C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

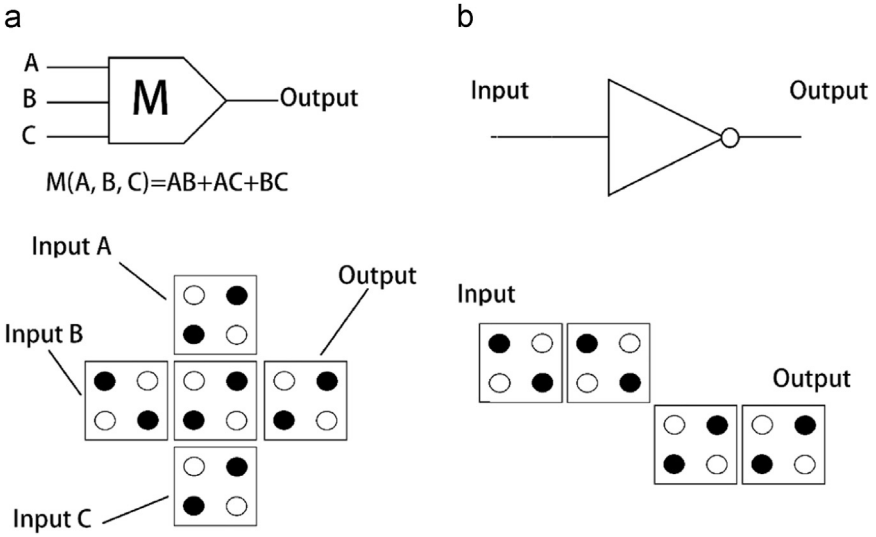

Fig. 2. Structure blocks of (a) majority gate and (b) inverter gate.